ESD in Automotive In-Vehicle Networks

SE IEEE EMC Society
Nexperia’s Contacts for ESD Protection

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Overview

- Motivation
- Datasheet Parameters and Selection Criteria for ESD Protection Devices
- ESD protection for
  - Classics: LIN/CAN, CAN-FD
  - Automotive Ethernet (OPEN Alliance)
  - High Speed Links
- Extra: How to simulate ESD?
ESD – Electro Static Discharge

**WHAT**
A sudden electrostatic discharge between persons, devices or components

**HOW**
- A charged person touches an integrated circuit (IC)
- A charged IC drops on a grounded metal plate
- A charged machine touches an IC
- An electrostatic field is induced by high voltages

**PROBLEM**
- Causing malfunction (*reversible* by power-off-on cycle)
- Destruction of electrical components (*irreversible*): gate oxide, metallisation or PN junctions
ESD – Electro Static Discharge

Device level

- ICs can be destroyed (ESD) during production (assembly, placement, handling)
- Qualification by standards (JEDEC)
  - Human Body Model (HBM), 2kV for IC pins
  - Machine Model (MM)
  - Charged Device Model (CDM)
- ESD pulses are given to all IC pins.
- ESD "on-chip protection" protects against defects during production.

System level

- Complete Systems (e.g. clusters, head units) can be destroyed by ESD during operation or service
- "System Level" ESD standards
  - IEC 61000-4-2
    Electrostatic discharge immunity test
    - ISO 10605
- ESD pulses are given to certain accessible interfaces. Individual components (e.g. ICs) are not tested!
- Special ESD Devices are added on the board to avoid destruction by ESD.
ESD – System Level Testing: IEC 61000-4-2

Typical waveform of ESD current

- Rise time
  - 0.7 – 1 ns (von 10% auf 90%)
- Peak current
  - +/- 10% tolerance
- Current after 30 ns
  - +/- 30% tolerance
- Current after 60 ns
  - +/- 30% tolerance

<table>
<thead>
<tr>
<th>Applied Voltage in kV</th>
<th>Peak Current Human Body Model in A</th>
<th>Peak Current IEC 61000-4-2 in A</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.33</td>
<td>7.5</td>
</tr>
<tr>
<td>4</td>
<td>2.66</td>
<td>15.0</td>
</tr>
<tr>
<td>6</td>
<td>4.00</td>
<td>22.5</td>
</tr>
<tr>
<td>8</td>
<td>5.33</td>
<td>30.0</td>
</tr>
<tr>
<td>10</td>
<td>6.66</td>
<td>37.5</td>
</tr>
</tbody>
</table>
System ESD Testing

Direct (contact) discharge:

6 to 15kV

Indirect discharge

≥15kV

Air discharge

Strongly dependent on the system.
ESD – Defects caused by ESD

Destruction mechanism

High voltage

High energy
ICs become more sensitive

Increased performance and density lower the SoC ESD robustness

- Gate thickness and chip size (channel length) decreases
- Maximum gate voltage decreases (e.g. for CMOS090 <1.5V static)
- New Processes are optimized for area and performance

HBM targets will be lowered
- HBM targets will be lowered to meet device level ESD robustness
- HBM target already lowered down to 1 kV
- This trend is applicable for CDM targets

IC robustness will decrease and require more dedicated discrete ESD solutions

Source:
ESDA, 2016
Duvvy/Miller, 2009
# Benefits of external ESD protection

Example CAN bus with PESD2IVN24-T

<table>
<thead>
<tr>
<th>IC/Transceiver</th>
<th>ESD robustness w/o PESD2IVN24-T</th>
<th>ESD robustness with PESD2IVN24-T</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLE 9263BQXV33XUMA1</td>
<td>+ 8 kV (HBM)</td>
<td>+ 30 kV</td>
</tr>
<tr>
<td>TLE 9262BQXXUMA1</td>
<td>+ 8 kV (HBM)</td>
<td>+ 30 kV</td>
</tr>
<tr>
<td>MCP25625 E/SS</td>
<td>+ 8 kV (HBM)</td>
<td>+ 30 kV</td>
</tr>
<tr>
<td>LPC11C22FBD48/301</td>
<td>+ 8 kV (HBM)</td>
<td>+ 30 kV</td>
</tr>
<tr>
<td>SN65HVD232QDRQ1</td>
<td>+ 11 kV (HBM)</td>
<td>+ 30 kV</td>
</tr>
<tr>
<td>TLE7250GXUMA1</td>
<td>+ 10 kV (HBM)</td>
<td>+ 30 kV</td>
</tr>
<tr>
<td>TJAA1042T/3,118</td>
<td>+ 12 kV (HBM)</td>
<td>+ 30 kV</td>
</tr>
<tr>
<td>TJAA1044T</td>
<td>+ 10 kV (HBM)</td>
<td>+ 30 kV</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>+30 kV</td>
</tr>
</tbody>
</table>

**Device level**

**System level**

External ESD Protection can handle **more ESD current** and can be chosen **application specific**.

Very Robust System in the Field!
Selection Criterion

Package (shape/size/footprint)

Side-wettable flanks for AOI

Number of signal lines
e.g. differential or single ended, one or more channels

Electrical performance

- Reverse stand-off voltage $V_{RWM}$
- Breakdown or trigger voltage $V_{br}$ or $V_t$
- Clamping voltage $V_{clamp}$
- Dynamic resistance $R_{dyn}$
- **Device capacitance $C_d$** and other parasitics
Characteristics of ESD Protections

Classical Zener Characteristic

\[ V_{RWM} \]: Reverse standoff voltage
\[ V_{BR} \]: Breakdown voltage
\[ V_{CL} \]: Clamping voltage
\[ I_{RM} \]: Maximum reverse current
\[ I_{PP} \]: Maximum surge current
Characteristics of new ESD Protections

Snap Back

\[ V_{RWM} \]: Reverse standoff voltage
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\[ V_t \]: Trigger voltage
\[ V_h \]: Holding voltage
Characteristics of new ESD Protections

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- $V_{RWM}$: Reverse standoff voltage
- $V_{BR}$: Breakdown voltage
- $V_{CL}$: Clamping voltage
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- $V_t$: Trigger voltage
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Characteristics of new ESD Protections

Snap Back

Reducing $V_{\text{CL}}$ -> Improving Robustness of the PHY

$V_{\text{RWM}}$: Reverse standoff voltage
$V_{\text{BR}}$: Breakdown voltage
$V_{\text{CL}}$: Clamping voltage
$I_{\text{RM}}$: Maximum reverse current
$I_{\text{PP}}$: Maximum surge current
$V_t$: Trigger voltage
$V_h$: Holding voltage
Example: Automotive Ethernet
Clamping performance and system robustness

ICs become more sensitive
Increased performance and density lower the SoC ESD robustness

- ICs becoming more sensitive
  - Gate thickness and chip size (channel length) decreases
  - Maximum gate voltage decreases (e.g. for CMOS 900 <1.8V static)
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IC robustness will decrease and require more dedicated discrete ESD solutions
Automotive ESD Protection
LIN/CAN

- Requirement for ESD protection depend on OEM (approval list)
- Emission and Immunity: DPI, Pulses, ESD
  (in combination with transceiver!)
- Common requirements:

<table>
<thead>
<tr>
<th></th>
<th>LIN</th>
<th>CAN HS</th>
<th>CAN FD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cd</td>
<td>30 ... 100pF</td>
<td>10 ... 30pF</td>
<td>3.5 ... 10 (30) pF</td>
</tr>
<tr>
<td>ΔCd/Cd</td>
<td>nA</td>
<td>typical &lt; 0.5% for modern devices</td>
<td></td>
</tr>
<tr>
<td>VRWM</td>
<td>12 V Board Net</td>
<td>24 V Board Net</td>
<td></td>
</tr>
<tr>
<td></td>
<td>&gt;24V ISO16750-2 (28V)</td>
<td>&gt;32V ISO16750-2</td>
<td></td>
</tr>
</tbody>
</table>
Automotive ESD Protection
Evolution of In-Vehicle Networking

1980s

1990s

2000s

2010s

2020s
Classic Ethernet vs. OPEN Alliance

**Classic Ethernet**

- ESD Protection behind DC block, CMC and in front of PHY

  - Dual sourcing of ESD protection critical, because TLP curves and turn on behaviour need to match
  - Internal protection of the PHY and external ESD protection cannot always be matched

**OPEN Alliance Ethernet**

- ESD Protection in front of DC Block, CMC and PHY

  - Dual sourcing of ESD protection uncritical, because ESD protection in front of DC block and CMC protect whole system
  - External ESD protection is decoupled from internal protection of the PHY. PESD2ETH1G-T matches with every PHY
100BASE-T1 concept comparison

Comparison of ESD protection concepts evaluated by EMI scanner

No Protection versus Classic Protection

- PHY
- Connector
- OA compliant ESD protection
- Classic ESD protection
100BASE-T1 concept comparison

Comparison of ESD protection concepts evaluated by EMI scanner

No Protection

Classic Protection

Connector

PHY

OA compliant ESD protection

Classic ESD protection
OPEN Alliance Spec. for ESD protection devices

General requirements

- General requirements
  - Bi-direction device, 15kV IEC, 1000 discharges
  - Trigger voltage > 100V, $V_{DC,max}$ > 24V

- Additional tests
  - Mixed mode S-parameter measurements
    - To evaluate transmission, symmetry, and mode conversion, replaces requirements on $C_p$ and matching
  - Damage from ESD
    - To verify degradation, first measure S-parameters, apply ESD (8kV) discharges, and check S-parameters again
  - ESD discharge current measurement
    - Quantification of the current that would flow into the PHY
  - Unwanted clamping
    - Evaluate impact of ESD device onto RF immunity testing
OPEN Alliance Spec. for ESD protection devices

Damage from ESD

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Automotive ESD Protection
Challenges for High-Speed Interfaces

ESD
- >8kV (15kV)
- Different requirement on $V_t$ and $V_h$
- Robust and reliable technology

Signal Integrity
- Small capacitance and other parasitics
- Routing
- Impedance
- $S$-parameter (also MM)

EMC
- Emission (CE, RE)
- Immunity (RI, Stripl., BCI, etc.)
- Pulses (e-car?)

Automotive Environment
- Temperature
- Humidity
- Vibrations
- AC Coupling in STP
- HV (e.g. 48V)
- ...

Semiconductor technology, HF analysis (S-Param, Eye Diagramm, TDR), ESD Simulation - SEED, High-Speed Packages
Parameters impacting Signal Integrity

Device Capacitance
- Semiconductor technology (SCR, open base, etc.)
- Capacitance matching

Package parasitics
- Package technology
- Package size

Routing
- Impedance mismatch
- Assymetries
- Pad discontinuity
Application overview: capacitance vs. data rate

High-speed requires low capacitance
Impact of Capacitance

S-Parameters

![S-Parameters Diagram]

Parameter Sweep
- ParamSweep
- Sweep1
- SweepVar="Cd"

![Parameter Sweep Diagram]

RL (dB)

Freq (GHz)

IL (dB)

Values:
- 0.2pF
- 0.5pF
- 1.0pF
- 1.5pF
ESD Protection Device
Measurement vs simulation of capacitor

Nexperia

PESD30VF1BL
Bidirectional ESD protection diode

9. Characteristics

Table 6. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RMS}$</td>
<td>reverse standoff voltage</td>
<td>$T_{a=25}^\circ$</td>
<td>-</td>
<td>-</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{B}$</td>
<td>breakdown voltage</td>
<td>$I_{B}=10\ mA$, $T_{a=25}^\circ$</td>
<td>31</td>
<td>34</td>
<td>39</td>
<td>V</td>
</tr>
<tr>
<td>$I_{ON}$</td>
<td>reverse leakage current</td>
<td>$V_{D}=30\ V$, $T_{a=25}^\circ$</td>
<td>-</td>
<td>-</td>
<td>0.1</td>
<td>mA</td>
</tr>
<tr>
<td>$C_D$</td>
<td>diode capacitance</td>
<td>$f=1\ MHz$, $V_{D}=0\ V$, $T_{a=25}^\circ$</td>
<td>-</td>
<td>0.27</td>
<td>0.4</td>
<td>pF</td>
</tr>
<tr>
<td>$V_{CL}$</td>
<td>clamping voltage</td>
<td>$I_{CL}=7.5\ mA$, $T_{a=25}^\circ$</td>
<td>(1)</td>
<td>0.9</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$R_{DF}$</td>
<td>dynamic resistance</td>
<td>$I_{D}=16\ A$, $T_{a=25}^\circ$</td>
<td>(2)</td>
<td>23</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$S_{-Par}$</th>
<th>Par (dB)</th>
<th>$0.27\ pF$ simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.27pF</td>
<td></td>
<td>(simulation)</td>
</tr>
</tbody>
</table>

Freq (GHz) vs $|S_{-Par}|$ (dB) plot

Measured $S_{-Par}$

Diagram showing $C_D = 0.27\ pF$ and measurement.

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Simulation of a High Speed Link
PHY – Cable – PHY

1. Simulate Rx/Tx system separately
2. Include cable
3. Include connector
Simulation of High Speed Links
S-parameters simulation in ADS

Lossy microstriplines (\(\approx 100\Omega\) differential)
\(\varepsilon_r = 4.6, \tan \delta = 0.02\)

Ideal system, not including e.g. cable and connector!
**Simulation of a High Speed Link**

**PHY – Cable – PHY: Results**

<table>
<thead>
<tr>
<th>S-param</th>
<th>(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured</td>
<td></td>
</tr>
<tr>
<td>Ideal</td>
<td></td>
</tr>
<tr>
<td>Real</td>
<td></td>
</tr>
</tbody>
</table>

The more real the simulation the less impact can be observed from a modern ESD protection device.
Signal Integrity
Eye Diagramm (Cd=0.17pF)

w/o ESD device

with ESD device
Package Aspects
Comparison of SOT23 and DFN1110D-3 with PESD2CANFD24Vx (C_d = 5.2 pF)

- Ca. 2 cm traces on FR4
- Dashed line: no footprint
- **Clear advantage of leadless package**

![DFN1110D-3 and SOT23 images]
Package aspects – Clamping behavior
For high-speed busses

- $R_{\text{dyn}}$ governs the clamping voltage in a quasi-static condition.
- The dynamic behavior is determined by inductances and turn-on behavior.
System Efficient ESD Design (SEED)

- SEED simulates residual currents and voltages at IC pins
- Dynamic models for ESD protection and common mode chokes for ADS and Spice
- Allows to pick best protection during system concept design and significantly improve system robustness
Conclusion

- ESD can irreversibly destruct any electronic system, especially sensitive in-vehicle networks
- External ESD Protection can increase the system robustness of your system significantly
- ESD protection devices must be chosen for each application specifically
- Dedicated ESD protection can improve the system robustness of High-Speed applications without compromising SI
- SEED simulations help to simplify the selection and design process
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<tr>
<th>Nexperia Internet</th>
<th>Documentation Center</th>
<th>Application Handbook</th>
<th>Lab support</th>
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<tr>
<td><strong><a href="http://www.nexperia.com">www.nexperia.com</a></strong></td>
<td><strong>Link Selection Guide</strong></td>
<td><strong>ESD</strong></td>
<td><strong>Automotive version available now!</strong></td>
</tr>
</tbody>
</table>

1. **Search Function**
   - Cross Reference
   - Parametric Search
   - Package Search

2. **Product Overview**
   - [Path to Datasheets, Product Brochures, Application Examples, ... ]
   - Overview on all our Discrete, Logic and MOSFET devices
     - Diodes & Transistors
     - **Protection & Filtering**
     - MOSFETs
     - Logic
     - Packages

- **ESD Fundamentals**
- **Measurements & Characterization**
- **Interfaces and applications**
- **English & Chinese version**
- **PDF & Hardcopy**

- Dedicated engineering team to support customer requests
- Solution investigation with various analysis tools especially
- TLP, EMI scan, SEED
- Contact us for details