Fundamentals and Advances in Power Integrity Analysis

Methods of Data Communication Systems

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Distinguished Lecturer
Power path

VRM

TX

RX

Signal path

Return path
Power delivery network
Power Noise on 3.3V Supply
Logic Noise Margins

high

low
Receiver Eye Diagram
Analysis Parameters

\[ V_{\text{noise}}(s) = Z_{\text{power}}(s) I_{\text{load}}(s) \]
Transient load current
PDN Characterization

Pin

Z_{\text{power}}

\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}
Planar Circuit Analysis
A Single Representative Port
\[ Z_{\text{target}} \leq \frac{V_{\text{noise}}(s)}{I_{\text{load}}(s)} \]
Side view of a PCB
Self-resonance of decoupling caps

\[ Z_c = R + sL + \frac{1}{sC} \]
\[ Z_{in}(s) = Z_{11}(s) - \frac{Z_{12}^2(s)}{Z_{22}(s) + Z_C(s)} \]

Impedance Increases with Spacing

Planar structure with infinite extension

\[ Z_{ij} = \frac{s \mu d}{\beta 2\pi r_i} \frac{H_0^{(2)}(\beta |r_i - r_j|) J_0(\beta r_j)}{H_1^{(2)}(\beta r_i)} \]
Practical Case
Objective Function for Optimization

\[
\bar{Z}_{in}(s) = \frac{1}{n_p} \sum_{k=1}^{n_p} Z_{in_k}(s)
\]
Relations for Multi-pin and capacitor configuration

\[
Z = \begin{bmatrix}
Z_{n_p \times n_p} & Z_{n_p \times n_c} \\
Z_{n_c \times n_p} & Z_{n_c \times n_c}
\end{bmatrix}
\]

\[
Z_{in} = z_{pp} - Z_{pm} \left[ Z_m + Z_c \right]^{-1} Z_{mp}
\]
24 power pin BGA with 18 caps
Total required capacitance 9uF
Required Total Capacitance

\[ C_{\text{total}} = \frac{I_{\text{load}}(s)}{sV_{\text{noise}}(s)} \]
Initial/Optimal Placement of 18 Capacitors for 24 Pins

Cap Value = 1\mu F

June 2019
All 18 optimized 1μF capacitors are inside BGA Pinfield
Initial/Optimized Placement of 18 Capacitors for 24 Pins

Cap Value = 380 nF

June 2019
Half of optimized 380nF capacitors are inside BGA Pinfield

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>10^6</th>
<th>10^7</th>
<th>10^8</th>
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<tr>
<td></td>
<td>10^{-2}</td>
<td>10^{-1}</td>
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June 2019