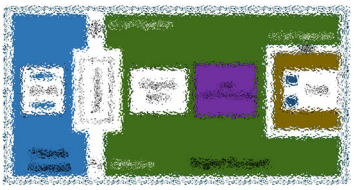
Horrible EMC Design Advice You Can Find on the Internet (and in Print)

Todd H. Hubing
Professor Emeritus
Clemson University

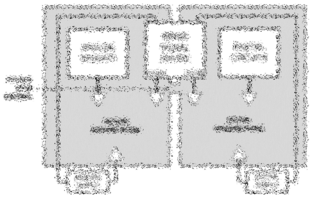
Learn to Recognize Bad Design Advice

Bad Layout Advice



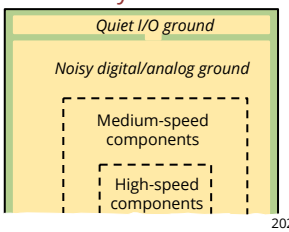
2022

Bad Grounding Advice



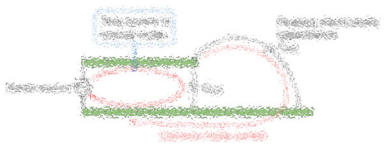
2022

Bad Layout Advice



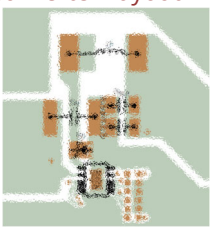
2023

Bad Information



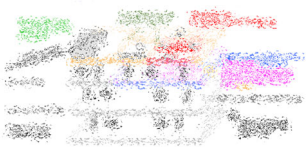
2023

Bad Converter Layout



2021

Bad Converter Stackup

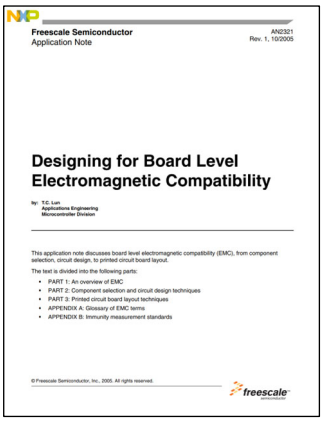


2023

2

Why is this happening?

- Companies are highly motivated to show up in web searches.
- Very little motivation to publish information that is accurate or relevant.
- No motivation to remove information that is dated or incorrect.


Freescale Semiconductor
Application Note
AN2321
Rev. 1, 10/2005

Designing for Board Level Electromagnetic Compatibility

by: T.C. Luo
Applications Engineering
Microcontroller Division

This application note discusses board level electromagnetic compatibility (EMC), from component selection, circuit design, to printed circuit board layout.

The text is divided into the following parts:

- PART 1: An overview of EMC
- PART 2: Component selection and circuit design techniques
- PART 3: Printed circuit board layout techniques
- APPENDIX A: Glossary of EMC terms
- APPENDIX B: Immunity measurement standards

freescale

3

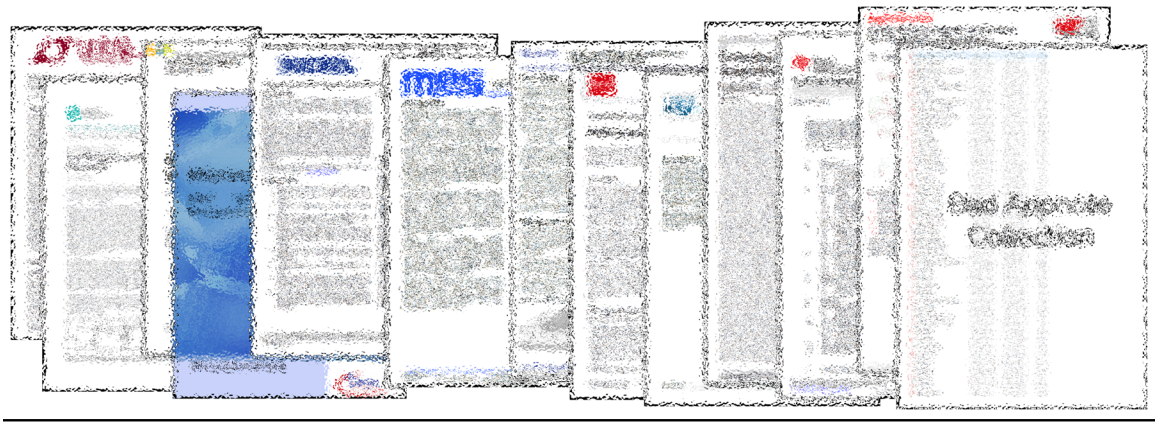
Why does this matter?

- It's costing companies time and money.
- It's reducing the reliability of electronic products.
- It makes people doubt that anyone really knows how to design a compliant product.
- It encourages a build-test-fix design mentality.

4

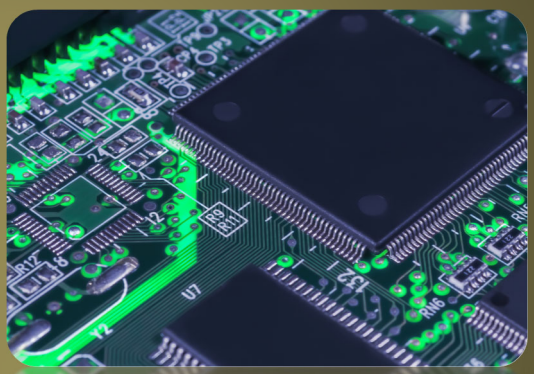
What can be done about it?

- Encourage the distribution of correct and relevant information.
- Promote discussion. Point out that the Emperor has no clothes.



5

Ground and Current Return



6

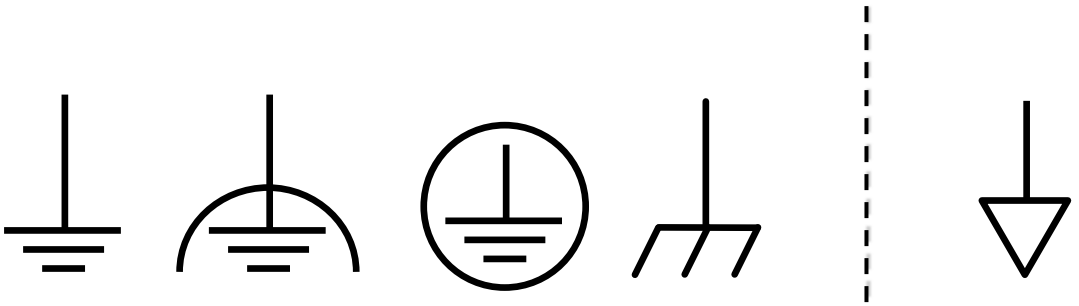
Things Labeled Ground

- Safety / Lightning Protection Conductors
- EMC Ground Structures
- Power and Signal ~~Current Returns~~

Current return is generally incompatible with grounding!!!

7

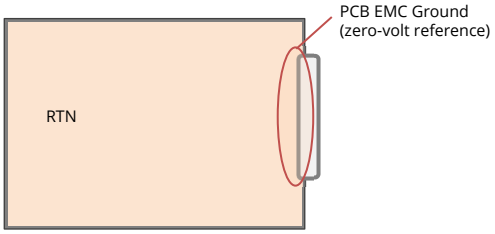
IEC 60417 Ground and Current Return Symbols



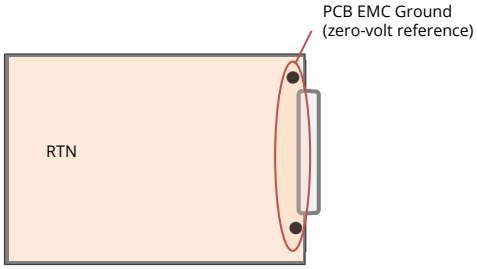
Earth Ground | Noiseless Earth Ground | Protective Earth Ground | Frame or Chassis Ground | Current Return

8

Where is the Circuit Board Ground?



PCB in product with no ground structure



PCB mounted near the ground structure

PCB ground cannot be at a different potential than the ground structure.

9

Quantifying Common-Impedance Coupling

Maximum common impedance coupling is easy to quantify!

$$V_{coupled} = I_{source} \times R_{shared}$$

(worst-case) (worst-case) (worst-case)

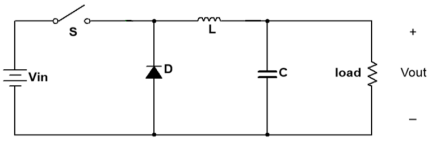
NOTE:
Use R_{shared}, not ωL_{shared} or $1/\omega C_{shared}$. Those values indicate magnetic- or electric-field coupling.

- Perform this calculation when you suspect conducted coupling will be an issue.
- ALWAYS perform this calculation before isolating signal returns labeled “ground”!

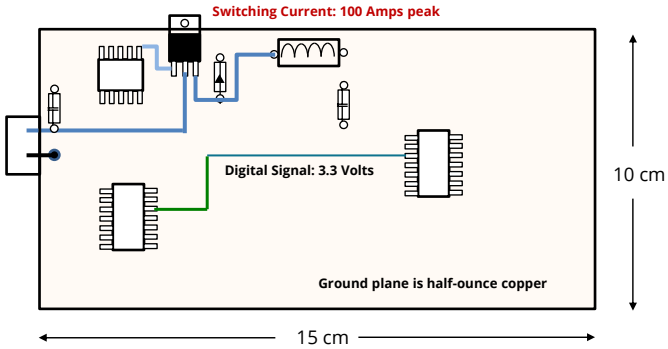
10

Isolate the Switching Current Loop?

Can the switching current share the ground plane with the digital circuits?



DC-DC buck converter



Don't neglect H-field coupling!

Resistance of board: < 1 mΩ/square

Voltage induced by common-impedance coupling: **< 100 mV**

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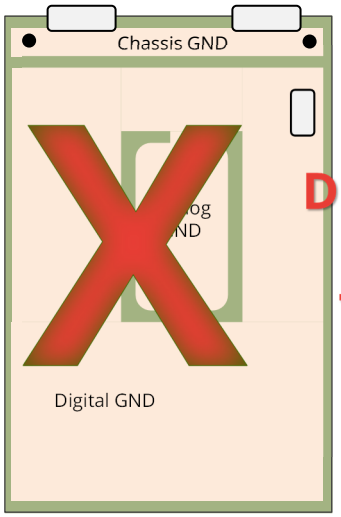
Vertical vs. Lateral Isolation



DO NOT DO THIS!

Lateral Isolation
can we guarantee that each attached cable is within 1 mV of the ground structure at radiated emissions frequencies?

Vertical Isolation
Provides low-frequency isolation, while facilitating high-frequency bonding.

- All planes that reference signals that leave the board should be tied to ground with capacitors.
- Only one plane usually needs to be full size.
- One or zero vias should connect planes with different labels.

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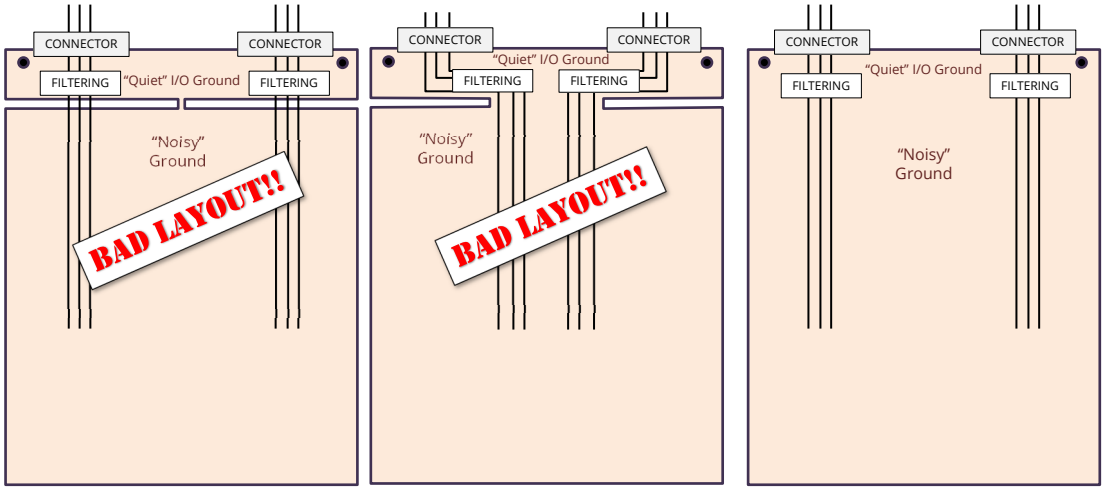
Two Bad Ground Plane Layouts (and one good one)



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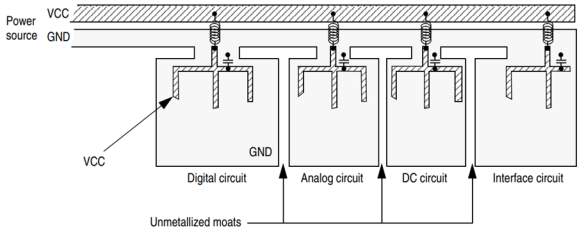
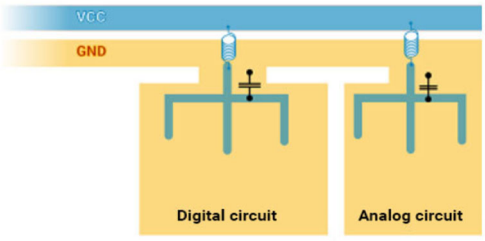
More Split Grounds

EMC at PCB Level: Potential Sources, Compliance, and Layout Techniques
Pan-European Training, August 2022



Sierra Circuits: December 2022



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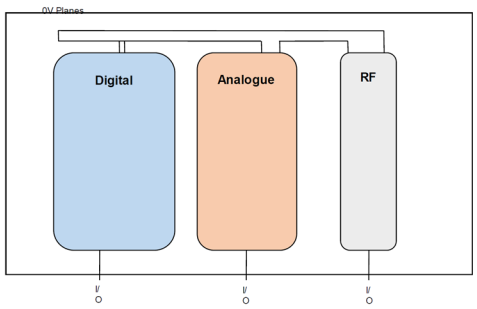
Electromagnetic Testing Services (Current Website)

DESIGN GUIDELINES
0V PLANES



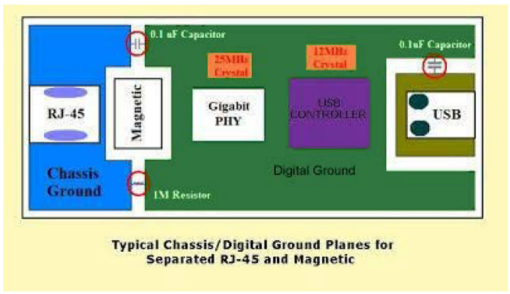
15

Sierra Circuits (January 2023)

Application Note: High-Speed PCB Design Guide

7.2.9 Ground Plane Isolation

Isolate the ground planes when required in the digital section. The figure presented below shows the necessity of isolation within the digital sections. The USB and RJ45 connectors communicate externally. The board GND needs to be isolated to avoid any noise or interference from external chassis/body GND.



Typical Chassis/Digital Ground Planes for Separated RJ-45 and Magnetic

RJ45 Connector and USB Connector

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Sierra Circuits (April 2023)

SIERRA CIRCUITS Best-in-Class PCB Fabrication, Assembly, & Components. Industry Leading PCB Designer's Tools.

PCB DESIGN | POWER INTEGRITY | SIGNAL INTEGRITY

Best PCB Grounding Techniques for High-Power and HDI Designs

What is the purpose of grounding in PCBs?

Ground provides a **common return path** for signals and power. It also serves as a **reference point in a circuit to measure voltages** across various points. Efficient grounding is quintessential for a safe operation of a circuit board. A robust ground system provides a solid foundation for a good power delivery network topology. In addition to this, it aids in thermal

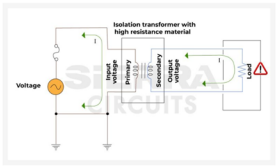
A single or multi-board electronic system needs a single common point for all grounds to come together. This can be a dedicated ground layer in your PCB or a chassis.

- Have separate grounds for input AC, unregulated, and regulated DC sections in power systems for good electrical isolation.
- Split planes must accommodate multiple power or ground nets carefully as they could inadvertently ruin or block a clear signal return path.
- Route the nets such that they do not intersect to avoid interference.
- Use stitching capacitors when the signal changes its ground reference.
- Use ground fill (copper pour) to achieve uniformity in the ground planes. These are then connected using vias.
- **Employ a common ground plane strategy** where the free space on a PCB is covered using copper pours.

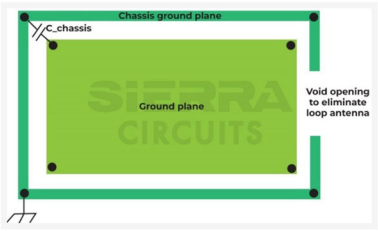
Floating reference

In an isolated system, the floating ground is a large reference conductor that is not physical connection to the earth. Hence, the voltage at the ground terminals and conductors is undetermined. The unintentional floating ground is considered a system fault, though in some cases it is intentionally used for safety.

For example, in the circuit below, isolation transformers are used in low-voltage (LV) power supplies to separate the main ground from the LV reference. The grounding current path from the main supply is avoided by floating the LV ground. Even if there is a fault on the LV side, it provides electrical safety.



Floating ground for safety using an isolation transformer



Elimination of ground loop antenna in chassis ground plane

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Sierra Circuits (April 2023)

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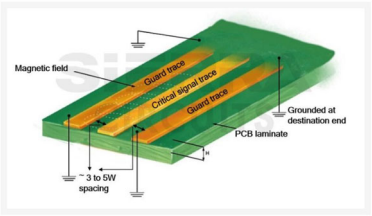
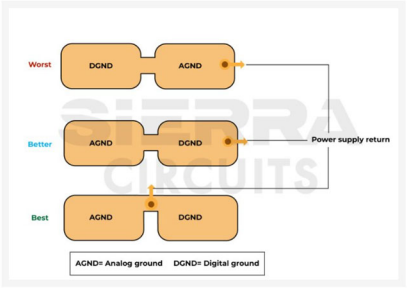
PCB DESIGN | POWER INTEGRITY | SIGNAL INTEGRITY

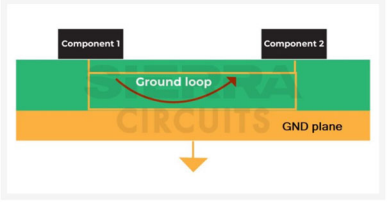
Best PCB Grounding Techniques for High-Power and HDI Designs



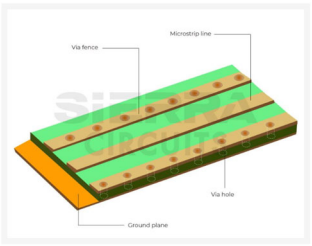
Guard traces for sensitive signals



PCB grounding techniques in mixed-signal circuits



Ground loop formed by two traces connecting to a ground plane



Via fencing

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Cadence Website (current)

Optimal EMI Filter PCB Layout Guidelines

CADENCE PCB SOLUTIONS

Stackup EMI Filter PCB Layout Guidelines for EMC and Manufacturability

1. Base the number of layers on pin density, the number of different types of signals, and provide good spacing between same type layers. For example, if possible, low and high frequency signal planes should be separate.
2. Do not place two signal layers adjacent to each other.
3. For vias, use correct aspect ratios and use the least complex to manufacture that meets your design requirements.
4. Apply good grounding techniques—for example, use separate planes for digital and analog signal types with a central point for board ground.
5. Ensure there is adequate minimal spacing between signal and ground planes.
6. Choose layer material thicknesses to meet impedance requirements.
7. Radiation creates heat. Therefore, incorporate adequate thermal dissipation techniques.

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Software Radius (Current Website)

13 PCB Layout Best Practices & Design Guidelines in 2023

Software Radius PCB DESIGN

13 PCB Layout Best Practices & Design Guidelines Every Engineer Needs to Know

Technique #11: Working With Mixed Signal Circuits

- *To ensure a good PCB design for those of you working with mixed signal circuits, try to ensure that you keep digital and analog ground planes separate.*

Similarly, while working with power circuits, it is better to keep the digital and analog grounds separate. The reason it is important to do so, is that voltage and current spikes from digital circuits might **generate noise** in analog circuits, which will have an impact on their performance.

If the situation requires you to place them together, it is recommended that you do so in the area of the supply path end, preferably in a point near the ground connection of the PCB. You might have other solutions to this; however, you can stick with this as a tried and tested method.

Technique #10: Bypass Capacitor Placement

The purpose of using Bypass capacitors is to have a filtering process for AC components and DC components. Additionally, they help in reducing noise, garbage signals, ripples and other such unwanted AC signals.

This is achieved by passing the AC fluctuations to the ground, and hence they are named bypass capacitors. As a general practice, you should connect the ground and wherever you wish to filter the voltage.

As a suggestion, you can place such a **capacitor at the board's power inlet**. The connecting wires in this region are long and receive numerous RF signals. Another application for these Bypass Capacitors could be near the ICs, and close to the ground and power pins, to filter out much of the noise that may be added internally on the board.

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FS Tech (April 2023)

FS TECH HOME SERVICES CAPABILITIES APPLICATION ABOUT REVIEWS BLOG

PCB Layout Design Tutorial Guide for Your Next Electronics Project

A printed circuit board (PCB) serves as a platform for connecting electronic components. Designers are required to adhere to DFM and IPC standards for circuit design to enhance the operational performance of the PCB. Nonetheless, designing a PCB is a complex task that demands extensive knowledge. In this tutorial, FS Technologies aims to provide essential **tips and rules** for PCB design that are vital for ensuring the functionality and reliability of the final product for your upcoming project.

Grounding Guidelines

- **Use a solid ground plane:** A solid ground plane provides a low-impedance return path for current, reduces noise, and improves the reliability of the circuit. Ideally, the ground plane should cover the entire PCB to ensure the current return path is always the shortest distance possible.
- **Keep high-speed signal return currents separate from other ground currents:** High-speed signals can create significant current loops that can interfere with other ground currents. To minimize this interference, it's important to keep high-speed signal return currents separate from other ground currents. This can be achieved by using a separate ground plane or by routing the high-speed signals and their return currents together.
- **Minimize ground loop area:** Ground loops can create unwanted noise in the circuit. To minimize the ground loop area, keep the ground path as short and direct as possible. Try to avoid routing ground traces in loops or using multiple ground points.
- **Separate analog and digital ground:** Analog and digital circuits should be kept separate to prevent interference. It's important to keep the analog and digital ground planes separate and to connect them at a single point to avoid ground loops. Separating analog and digital ground can help reduce crosstalk, noise, and interference.
- **Consider grounding for power supplies:** Power supplies should be properly grounded to minimize noise and interference. Use a separate ground connection for each power supply and connect them to the main ground at a single point. It's important to avoid sharing a ground connection between different power supplies as it can create ground loops and introduce noise into the circuit. Proper grounding can improve the performance and reliability of the circuit.

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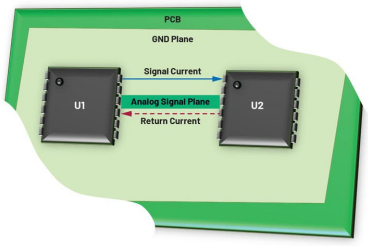
Article in Electronic Design Magazine (April 2023)

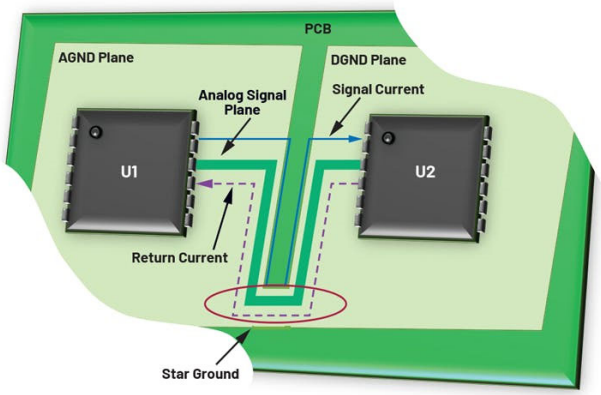
TECHNOLOGIES › ANALOG

Basic Guidelines for Mixed-Signal PCB Layout Design

April 6, 2023

This article presents a practical approach to the layout design of mixed-signal boards, discussing component placement, board layering, and ground-plane considerations.





Same article appears as an Analog Devices App Note dated September 2022

- It's useful to provide pads and vias so that the analog and digital ground planes can be connected, if necessary.

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Infineon (April 2023)

Hardware design guide for the PSoC™ 4 HV PA family

10.3 Ground and power supply

In general, the corresponding VDD and VSS lines should not be routed in chains, but in star shape.
Figure 20 shows an example of a bad and a good power line routing.

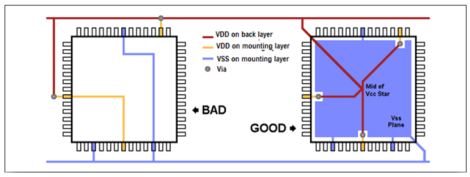

Figure 20 Generic example of bad vs. good power line routing

- Make sure that only one common star point connects analog and digital ground planes to each other. To have less noise on the analog part, the star point should be placed as far as possible from the MCU and as close as possible to the voltage regulator capacitor to the Electronic Control Unit (ECU) connector.
- Make sure that the digital and analog planes do not overlap and interfere. Furthermore, there should be no signal plane between these planes.
- Shield the analog input signals by the analog ground as much as possible.
- Avoid ground loops.

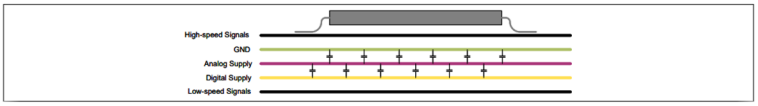

Figure 21 Example of a bad PCB layer stack

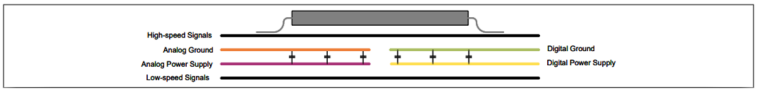

Figure 22 Example of a good PCB layer stack

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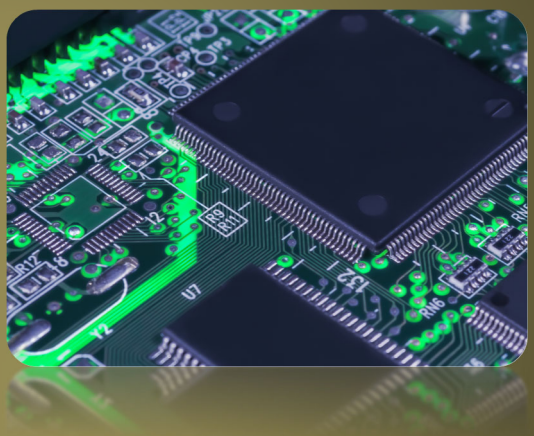
Circuit Board Decoupling



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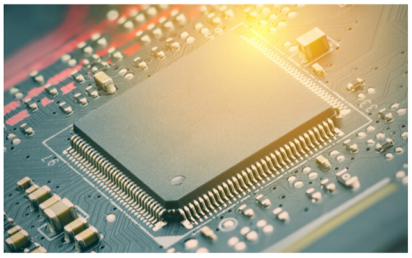
Cadence PCB Solutions (October 2020)

Where To Place Decoupling Capacitors?

Unlike finding the best spot for a modern vase, placing decoupling capacitors is easier.

The golden rule of decoupling capacitor placement is to minimize the distance between the component's voltage pin and the capacitor. This means you'll need to place the decoupling capacitor as close as possible to the IC's pin. If you're designing a multilayer PCB, place the capacitor beneath the component's pad. On a single-layer design, the capacitor is placed near to the pin and routed with a short trace.



Place decoupling capacitors close to voltage pins.

As mentioned, you'll need a 10uF and a 100 nF capacitor to stabilize against low and high-frequency fluctuations. The 100 nF capacitor should be placed closest to the voltage pin followed by the 10 uF capacitor. Repeat the process for as many VDD pin on the IC. There are some cases where the lack of space prevents the 1 decoupling capacitor per pin principle. In such instances, you'll still need a minimum of 1 decoupling capacitor per component.

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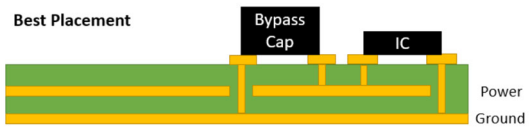
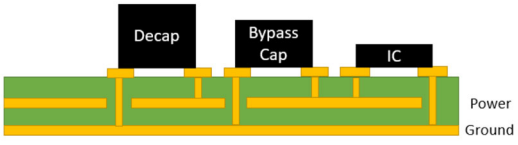
Altium (September 2020)

Decoupling Capacitor and Bypass Placement Guidelines



Typical bypass capacitor placement near an IC.



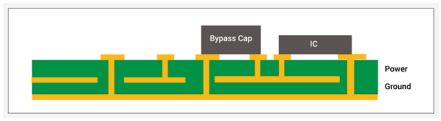
Typical decoupling capacitor and bypass capacitor placement.

Understanding the Relationship Between Frequency and Capacitor Size

When planning your designs it's important to keep in mind the inverse relationship between the frequency of the ripple (or current variation) and the capacitor size. If you know what this ripple looks like, you should be able to effectively map out the necessary capacitor size. For more complex ripples, you may need to employ different power supply bypass capacitors for the different frequencies you're dealing with.

26

What is a bypass capacitor?

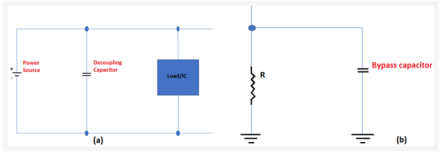


Bypass capacitor placement

A bypass capacitor is used to prevent noise from entering the system by bypassing it to the ground. It is connected between the supply voltage (Vcc) and ground (GND) pins to reduce power supply noise and voltage spikes on the supply lines.

What is the difference between decoupling and bypass capacitor?

Decoupling capacitor stores energy and dissipates it back into the power rail to maintain the smooth flow of current. The bypass capacitor provides the AC signal return path to switch between the power and ground rail.

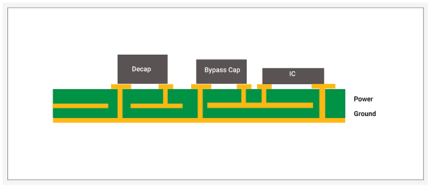


Difference between decoupling and bypass capacitor.

Considering their purpose and function, both bypass and decoupling capacitors can be used interchangeably. When powering any device, the primary objective is to provide a very low impedance path with respect to the input power ground. Some of the few noticeable differences are:

- Bypass capacitors are used to provide a low impedance shunt path to the high-frequency noise signals. They ensure high-frequency noise is mitigated before it flows into the entire circuit, resulting in circuit malfunction and an EMI problem. On the other hand, decoupling capacitors are used to stabilize the voltage variations.
- For the function of low impedance shunting, a single electrolytic capacitor is sufficient, but for stabilizing the signal, two different types of capacitors are required.

What is a decoupling capacitor?



Decoupling capacitor placement

What is the purpose of a decoupling capacitor?

Decoupling capacitors are used to isolate or decouple two circuits. In other words, they decouple AC signals from DC signals or vice versa.

- In case of input voltage drop, it provides adequate power to an IC to maintain the voltage level.
- In case of voltage surge, a decoupling capacitor prevents the excess current from flowing through the IC to keep the voltage stable.

2023 PCB Tips Brochure
SIERRA CIRCUITS

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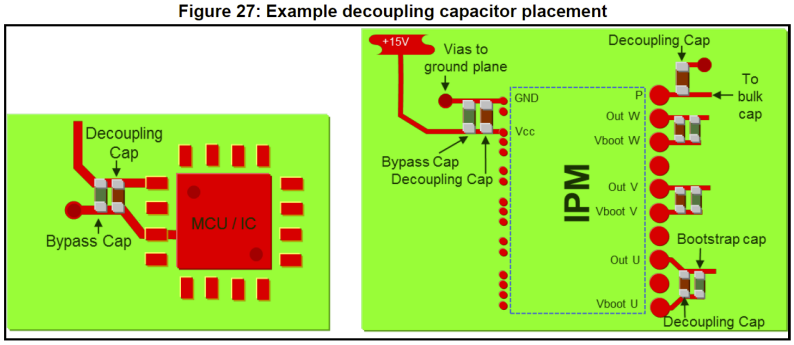
ST Microelectronics (2015)

Application Note: AN4694

Figure 27: Example decoupling capacitor placement



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How do you choose the value of a decoupling capacitor?

The number of capacitors to be used in a circuit depends on the number of power and ground pins and I/O signals present. Choose decoupling capacitors with sufficiently high self-resonant frequencies based on the signal bandwidth or operating frequency.

Understand the self-resonant frequency: The capacitor remains capacitive up to this frequency and starts to appear as an inductor above this frequency. The impedance of a decoupling capacitor reaches the minimum impedance at the frequency ω =1 / √LC. T
capacitor.

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Lower capacitance and lower inductanc
achieved by selecting a smaller surface-r
has lower parasitic inductance.

The low-frequency noise decoupling cap
noise should lie between 0.01 µF to 0.1 µF

- **Low equivalent series resistance (**
needs to provide current quickly, ch
- **Smaller package size:** Compact ca
the inductance.

How to choose the size of a decoupling capacitor for digital PDN?

The size of the decoupling capacitor is evaluated based on the impedance of the power distribution network (PDN) and the charge required by the switching IC. Evaluating accurate capacitor size and placing it correctly helps to reduce ripples and noise on the PDN.

$$C = \frac{\Delta I \cdot T_{rise}}{2V_{IC}}$$

Calculating decoupling capacitor size based on the current dr

Where: T_{rise} is the rise time, V_{IC} is the IC voltage, and ΔI is the c

Note: The above formula is valid if the signal bandwidth is less
decoupling capacitor. Signal bandwidth is given by: (0.35/signa

How to choose the size of a decoupling capacitor f

When providing stable power for an analog IC, the decoupling
provide stable power as an analog IC operates.

The size of the decoupling capacitor for an analog IC is give

$$C = \frac{I}{2\pi f V_{IC}}$$

The current drawn by the IC would be an increasing function

Where: f is the frequency, V_{IC} is the IC voltage, and I is the curr

How to choose the size of a decoupling capacitor based on PDN impedance?

Decoupling capacitors provide the required charge in a timely manner and reduce the output impedance of the overall PDN. Practically, a it is only effective over a particular frequency range. Its impedance decreases linearly with the decrease in frequency and increases with the increase in frequency. This increase in the impedance of a practical decoupling capacitor is due to the its parasitic inductance.

Also read, How to reduce parasitic capacitance in PCB layout.

One of the best ways to determine decoupling capacitor size is based on the target PDN impedance.

$$C = \frac{V_{ripple}(C)}{2\pi f V_{IC} Z_{PDN}(C, f)}$$

Its size is based on the required voltage ripple, target PDN impedance, and target PDN voltage.

Where: f is the frequency, V_{IC} is the IC voltage, V_{ripple} is the voltage ripple, and Z_{PDN} is the target PDN impedance.

Target PDN impedance and the PDN ripple voltage are functions of the capacitance, making it a very complex problem to solve. Calculating 'C' requires several iterations. The above equation is more accurate because it can incorporate the effect of the resonance frequency of the decoupling capacitor and resonances that arise due to parasitics in the PCB layout.

While calculating Z_{PDN} for different values of C and f, we arrive at the best values of C to get the lowest Z_{PDN} for all the frequency ranges.

Note: The exact value of the decoupling capacitors to be used is always provided with the ICs datasheet.

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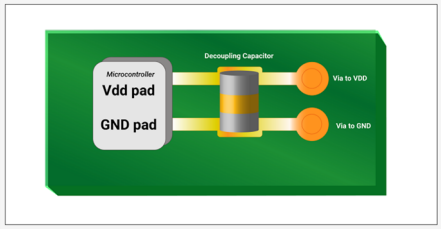
Sierra Circuits (December 2022)



Power rail noise is reduced by placing the decoupling capacitors close to the IC power pins.

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Sintecs (January 2023)

7. **Place decoupling capacitors to reduce noise**: a simple rule for capacitor placement is to use the 20th wavelength of the transistor switching speed. The capacitor should be as close as possible to the IC for a short travel time.

8. **Use signal termination strategies to reduce EMI problems**: If the distance between the driver and the receiver is more than a quarter of the wavelength, it will cause ringing. To mitigate this, place a series resistor within the lump distance.
9. **Don't rely only on simulation tools**: one of the challenges with EMC simulation tools is that they may not always be 100% precise. Sometimes a simulation may indicate that your design is perfect, but in reality, the system may still fail.

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Renesas (August 2022)

VersaClock7 PCB Layout Guidelines

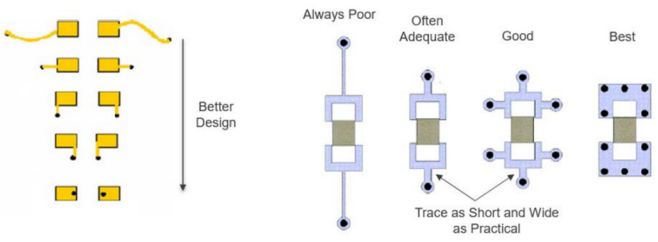

Figure 17. Decoupling Capacitor Pad Design

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Infineon (April 2023)

Hardware design guide for the PSoC™ 4 HV PA family

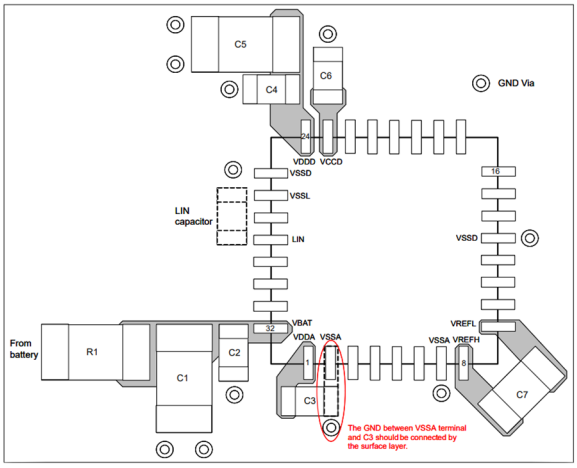
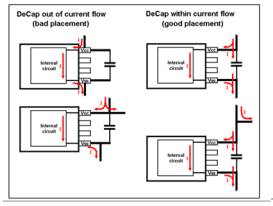
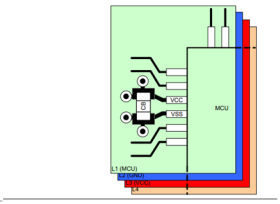


Figure 2 **PSoC™ 4 HV PA power supply block layout**



Power supply decoupling capacitor placement



Recommended power supply decoupling on boards

Symbol	Overview	Parameter		
		Value 1	Value 2	Remark
C1	Decoupling/smoothing capacitor for high voltage domain	2.2 µF X7R	> 50 V	Smoothing capacitor for battery input.
C2	Decoupling capacitor for high voltage domain	0.1 µF X7R	> 50 V	Decoupling capacitor for battery input. Place as close as possible to the VBAT pin.
C3	Decoupling capacitor for VDDA domain	0.15 µF X7R	> 6.3 V	Decoupling capacitor for internal analog power supply. Place as close as possible to the VDDA and VSSA pin.
C4	Decoupling capacitor for VDDD domain	0.1 µF X7R	> 6.3 V	Decoupling capacitor for internal digital power supply. Place as close as possible to the VDDD and VSSD pin.
C5	Decoupling/smoothing capacitor for VDDD domain	3.3 µF X7R	> 6.3 V	Decoupling capacitor for internal digital power supply. Place it next to C4.

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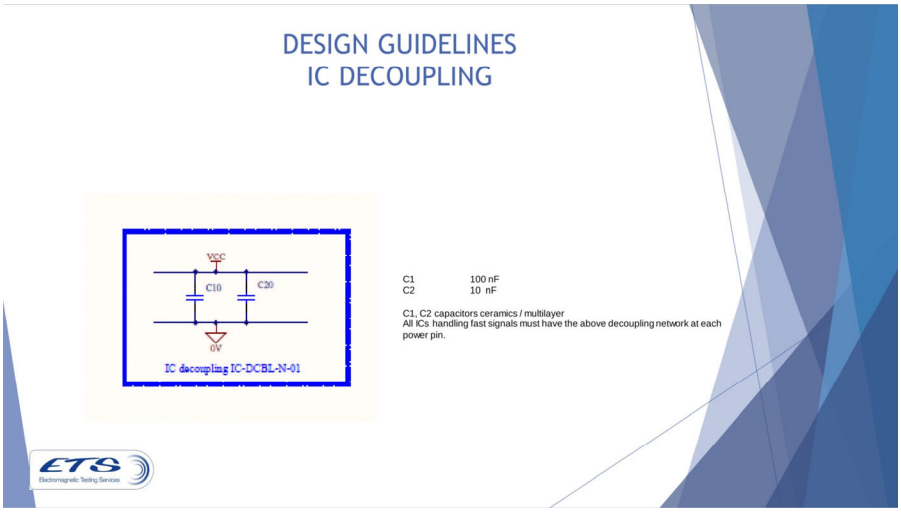
Electromagnetic Testing Services



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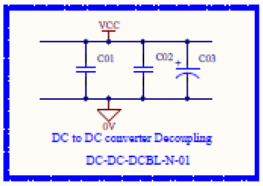
Electromagnetic Testing Services

DESIGN GUIDELINES
DC to DC Converter Decoupling Network



C1 100 nF
C2 10 nF
C3 100uF

C1, C2 capacitors ceramics / multilayer
C3 electrolytic reservoir low ESR

Add to all inputs and outputs of DC-DC converters

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Texas Instruments (April 2023)

TEXAS INSTRUMENTS
MSPM0L1306, MSPM0L1305, MSPM0L1304, MSPM0L1303
SLASEX0B – OCTOBER 2022 – REVISED APRIL 2023

MSPM0L130x Mixed-Signal Microcontrollers

1 Features

- **Core**
  - Arm® 32-bit Cortex®-M0+ CPU, frequency up to 32 MHz
- **Operating characteristics**
  - Extended temperature: –40°C to 125°C
  - Wide supply voltage range: 1.62 V to 3.6 V
- **Memories**
  - Two I²C interfaces; one supports FM+ (1 Mbit/s) and both support SMBus, PMBus, and wakeup from STOP
  - One SPI supports up to 16 Mbit/s
- **Clock system**
  - Internal 4- to 32-MHz oscillator with ±1.2% accuracy (SYSOSC)
  - Internal 32-kHz low-frequency oscillator with ±3% accuracy (LFOSC)

TI recommends connecting a combination of a 10-µF and a 0.1-µF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10-µF bulk decoupling capacitor is a recommended value for most applications, but this capacitance may be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

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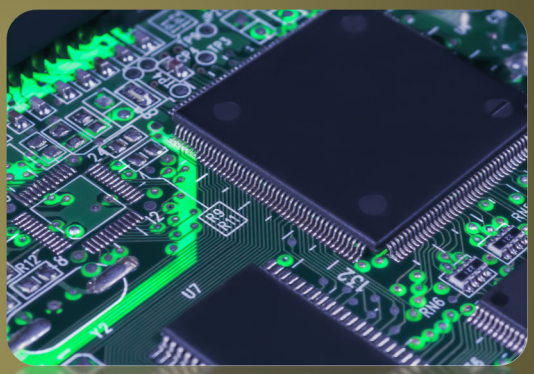
Filter Design



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Würth Elektronik (December 2017)

Application Note: ANP044c

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

WÜRTH ELEKTRONIK

2.5. CIRCUIT DIAGRAM „BETTER“ DESIGN (DESIGN 2)

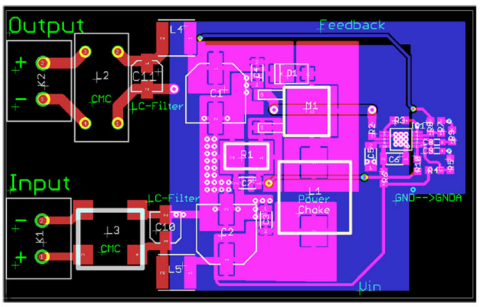

Fig. 16: Circuit-board layout of the good design (Design 2)

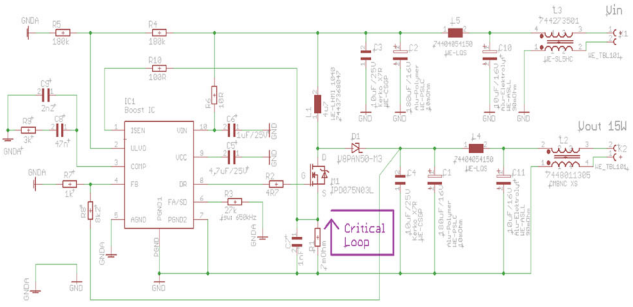

Fig. 15: Circuit diagram of a good design (Design 2) with Uin = 9 V, Uout = 12 V, Iout = 1.25 A, fsw = 650 kHz

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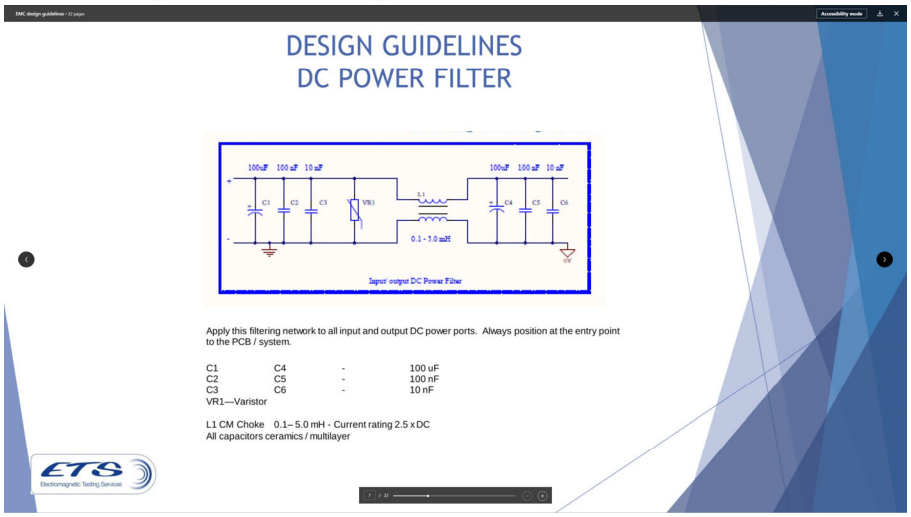
Electromagnetic Testing Services



GaN Gate Driver - 2019

Typical Application (continued)

For more extreme cases or where no delay is tolerable, using a common-mode choke provides the best results. One example application where the ground bounce is particularly challenging is when using a current sense resistor. In this application, the LMG1210 ground is connected to the GaN source, while the controller ground is connected to the other side of the current sense resistor as shown in Figure 18.

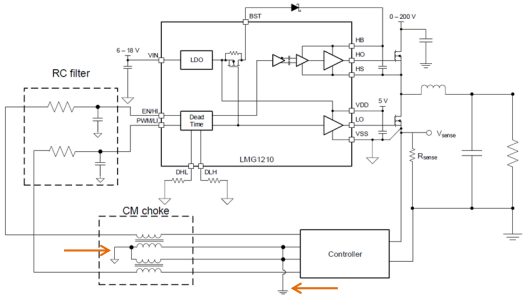
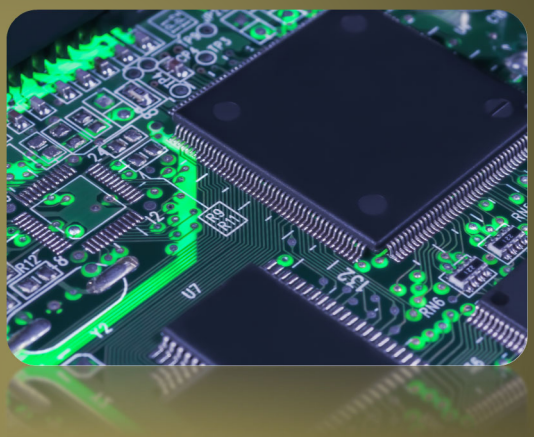


Figure 18. LMG1210 Configured With Current Sense Resistor Using a CMC as Filter

The combination of high dI/dt experienced through the sense resistor inductance will cause severe ground noise that could cause false triggering or even damage the part. To prevent this, a common-mode choke (CMC) can be used. Each signal requires its own CMC. Also, to provide additional RC filtering, a 100 Ω resistor should be added to the signal output line before the LMG1210.

Power Converter Layout



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Linear Technologies (2012)

Application Note: AN139

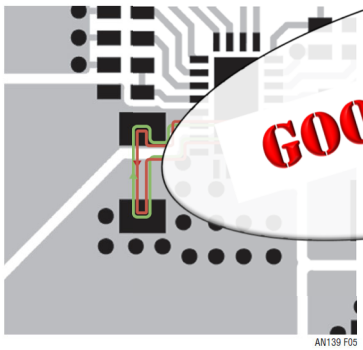

Figure 5

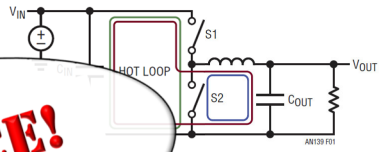

Figure 1

GOOD ADVICE!

During the on cycle with S1 closed and S2 open, the AC current follows the red loop (Figure 1). During the off cycle, with S1 open and S2 closed, the AC current follows the blue loop. Both currents have a trapeze shape. People often have difficulty grasping that the loop producing the highest EMI is not the red nor the blue loop. Only in the green loop flows a fully switched AC current, switched from zero to I_{PEAK} and back to zero. We refer to the green loop as a hot loop, since it has the highest AC and EMI energy.

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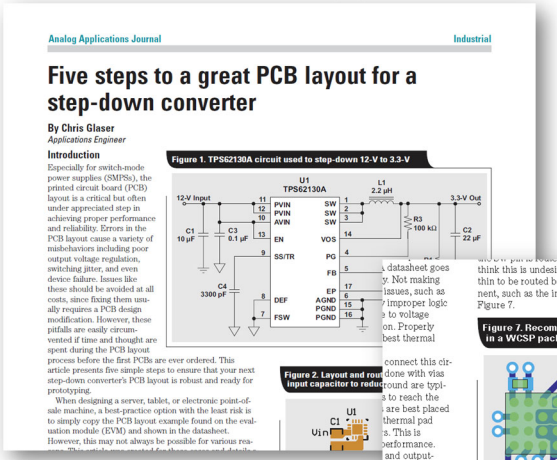
Texas Instruments Application Note



Analog Applications Journal — Industrial

Five steps to a great PCB layout for a step-down converter

By Chris Glaser
Applications Engineer

Introduction

Especially for switch-mode power supplies (SMPSs), the printed circuit board (PCB) layout is a critical but often under appreciated step in achieving proper performance and reliability. Errors in the PCB layout cause a variety of misbehaviors including poor output voltage regulation, switching jitter, and even device failure. Issues like these should be avoided at all costs, since fixing them usually requires a PCB design modification. However, these pitfalls are easily circumvented if time and thought are spent during the PCB layout process before the first PCBs are ever ordered. This article presents five simple steps to ensure that your next step-down converter's PCB layout is robust and ready for prototyping.

When designing a server, tablet, or electronic point-of-sale machine, a best-practice option with the least risk is to simply copy the PCB layout example found on the evaluation module (EVM) and shown in the datasheet. However, this may not always be possible for various rea-

Figure 1. TPS62130A circuit used to step-down 12-V to 3.3-V

datasheet goes
y. Not making
issues, such as
improper logic
to voltage
on. Properly
best thermal
connect this cir-
done with vias
ound are typi-
to reach the
are best placed
thermal pad
s. This is
performance.
and output-
nto the system
onents is not
ouple noise from
rounds are best
ere they make a
ermal pad.

think this is undesirable because that trace must be rather thin to be routed between the terminals of a small component, such as the input capacitor. This then looks like Figure 7.

Figure 7. Recommended layout of the TPS62360 in a WCSP package[2]

App Note: AAJ 1Q 2015

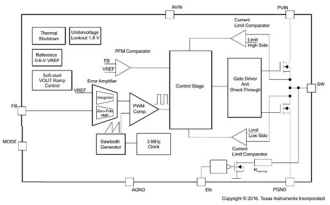
For Step-Down Converters

Note that HF current will not flow on isolated PGND. Path of least inductance takes it back to main ground plane.

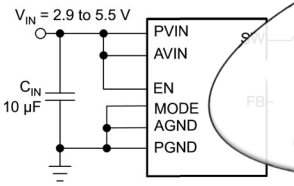
Single-point current return?!!

TLV62065 DC/DC Buck Converter (Data Sheet)

Automotive 2.9V to 5.5V, 3 MHz, 2A



Typical Application Circuit



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GOOD ADVICE!

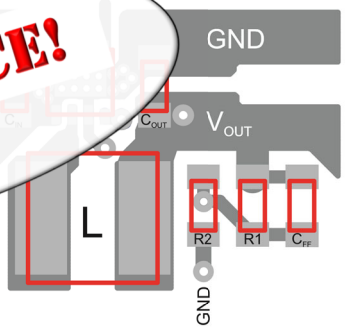

Figure 24. PCB Layout

Be sure that vias to GND and any voltage planes are adjacent to capacitor mounting pads!

ROHM Semiconductor (2017)

Application Note: AN066E

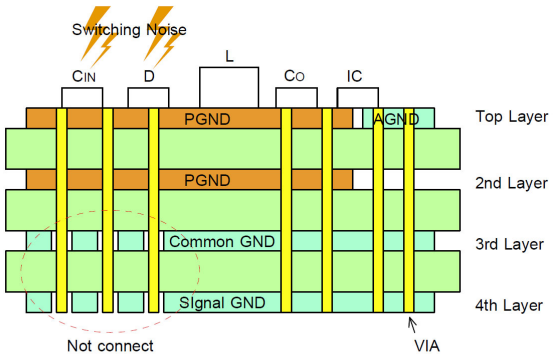

Figure 9. Power ground connecting method for multilayer board

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MPS (2023)

PCB Design for Low-EMI DC/DC Converters

Since the GND copper area under the DC/DC circuit has impedance, the high di/dt eddy currents create potential differences and make the area noisy. This noisy GND area must be separated from the system GND area, especially from any GND reference for filters and connectors. In a multi-layer PCB, these are separated by shaping the individual layers and by the impedance of the connecting vias between them.

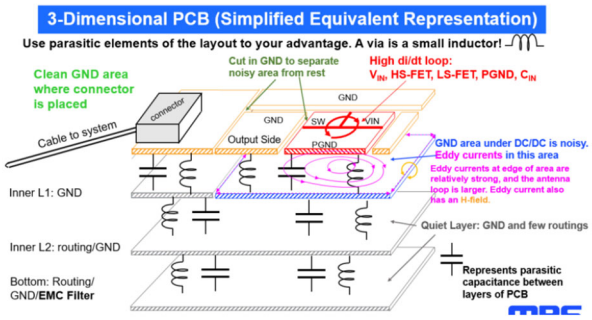

Figure 2: 3-Dimensional PCB View – Layout is Part of the Circuit

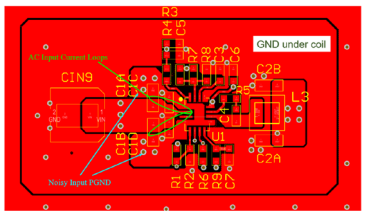

Figure 5: MPQ4430 PCB Top-Side Layout

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Analog Devices Application Note (January 2021)

AN-1119: Printed Circuit Board Layout Guidelines for Step-Down Regulators, Optimizing for Low Noise Design with Dual Channel Switching Controllers

Note: This is a Buck converter operating at 200 kHz to 1.5 MHz.

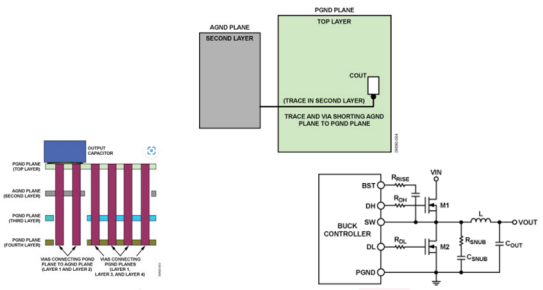
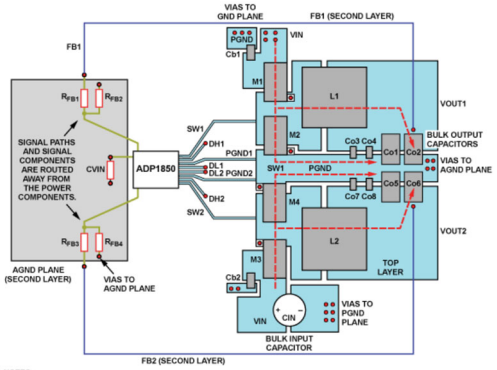


Figure 6. Snubber and Gate Resistance Circuit



NOTES
1. LAYER 1: SIGNAL AND HIGH CURRENT PATHS.
2. LAYER 2: AGND PLANE.
3. LAYER 3 AND 4: PGND PLANES. M1 AND M2 ARE SUPERSO8 PACKAGES HIGH-SIDE AND LOW-SIDE MOSFETs FOR REGULATOR 1, RESPECTIVELY. SIMILARLY, M3 AND M4 ARE FOR REGULATOR 2. Co1 TO Co8 ARE OUTPUT CAPACITORS. CIN IS THE INPUT BULK CAPACITOR. Cb1 AND Cb2 ARE BYPASS MULTILAYER CERAMIC CAPACITORS (MLCC).

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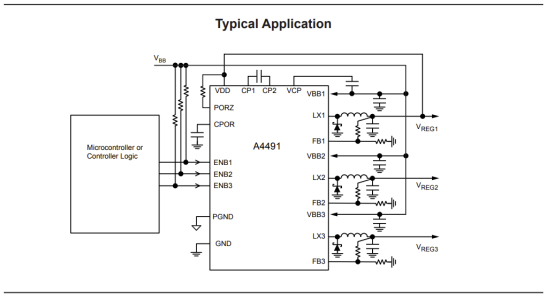
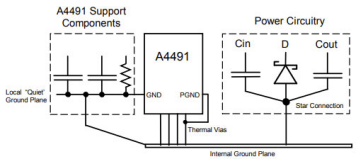
Allegro (February 2022)

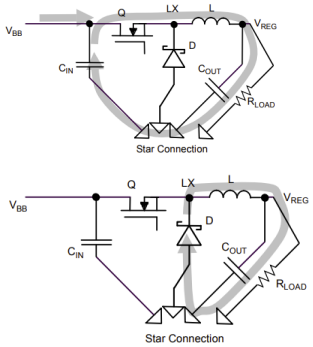
Allegro A4491 (Triple Buck Converter)

- 1 – 5 V from 4.5 – 23 V
- 1.5 A each
- 550 kHz

- Interleaved Turn-On Cycles







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Vicor (January 2022)

Data Sheet: Vicor ZVS Regulators (PI34xx-LGIZ)

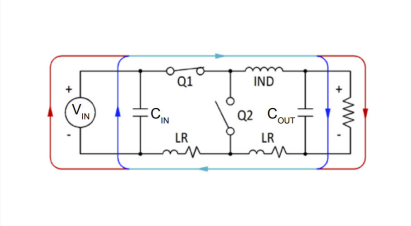


Figure 20 *— Typical buck regulator*

The path between the C_{OUT} and C_{IN} capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on.

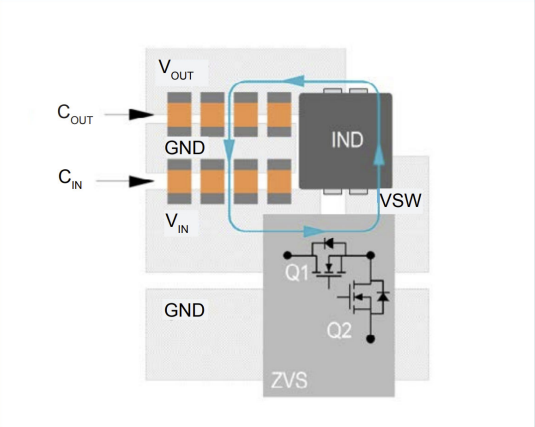


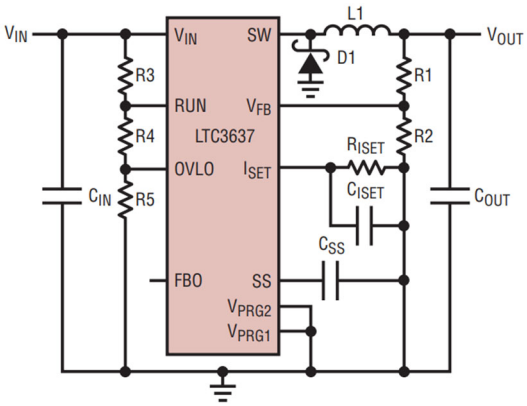
Figure 23 *— Recommended component placement and metal routing*

49

Analog Devices (2022)

Data Sheet: LTC3637-D

Analog Devices 11/2022



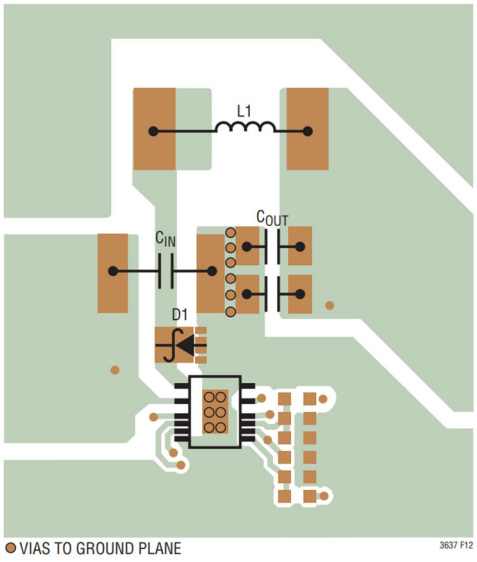


Figure 12. Example PCB Layout

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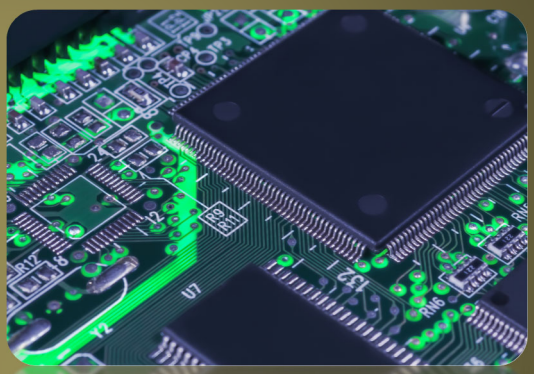
Power Inverter



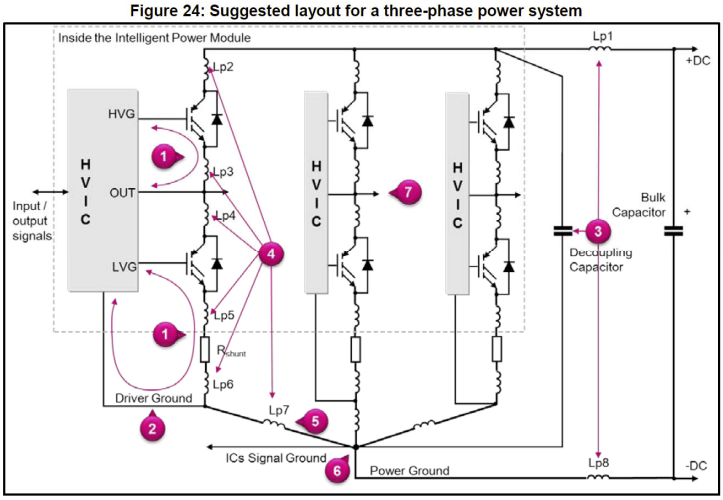
51

ST Microelectronics (June 2015)

Application Note: AN4694

Any time you see currents being routed to a single point; someone has confused the concept of ground with the concept of current-return.

Figure 24: Suggested layout for a three-phase power system



"6. Connecting the signal ground to the three driver grounds through a star connection improves the balance and symmetry of the three-phase driving topology."

52

Texas Instruments (October 2021)

Application Note

Best Practices for Board Layout of Motor Drivers

Texas Instruments

Motor Drive Business Unit

ABSTRACT

PCB design of motor drive systems is not trivial and requires special considerations and techniques to achieve the best performance. Power efficiency, high-speed switching frequency, low-noise jitter, and compact board design are few primary factors that designers must consider when laying out a motor drive system. Texas

1.2 Using a Ground Plane

In a 4-layer board or a larger 2-layer board design, it is recommend to use a ground plane. Having one layer of the PCB as a continuous ground plane lets each signal have the shortest return path and decreases coupling and interference. It is recommended to minimize ground plane discontinuity by carefully routing signal traces, and place vias away from each other to prevent breaks in the plane. For more information on via placement, see Section 2.4.

Most DRV devices have a thermal pad that functions as a ground and use the ground copper to sink heat. Figure 1-4 shows good layout examples for common and split ground planes.

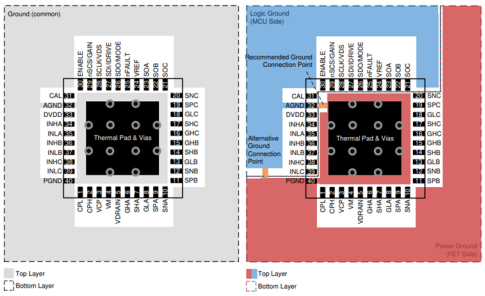


Figure 1-4. Common Ground Plane vs Split Ground Plane

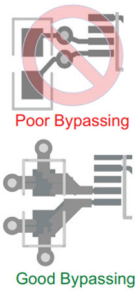


Figure 5-5. Bypass Capacitor Placement

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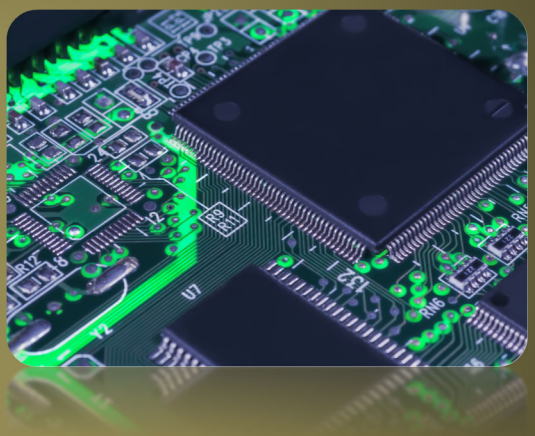
One More Thing!



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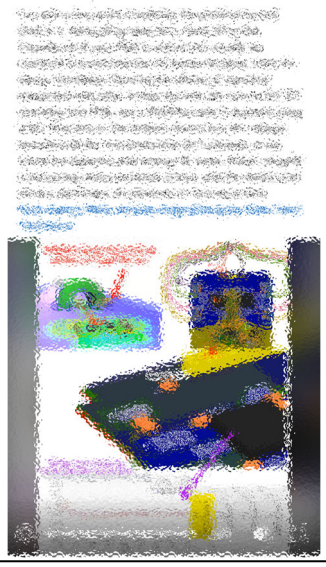
An Alarming Trend



Design Rules Based on Simulations

Conclusion was that decoupling capacitor location and value matter.
(This is sometimes true, but often false.)

Output is not a 300 MHz sine wave

No stackup information

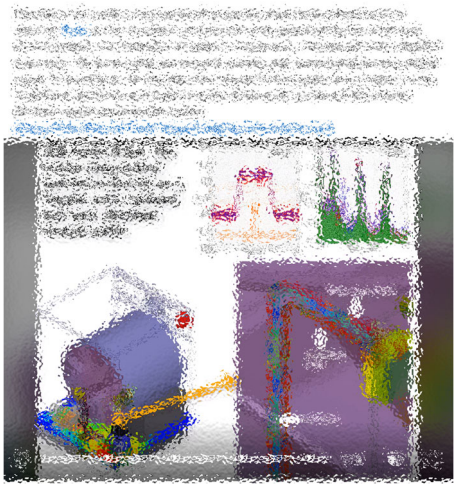
No decoupling geometry or design information

Where are the ports?

No reference, no model information.

55

An Alarming Trend



Design Rules Based on Simulations

Conclusion was that "in terms of immunity to external EMI" a twisted pair is better than a "regular wire" but not as good as a coaxial cable.
(This is clearly false!)

It wasn't clear what type of coupling was involved

Not clear what the criteria was.

Virtually no information model information is provided.

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