How to Keep Your Boards from Screaming Like a Banshee

Practical design guidelines for lower switching noise and EMI

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About the Eric

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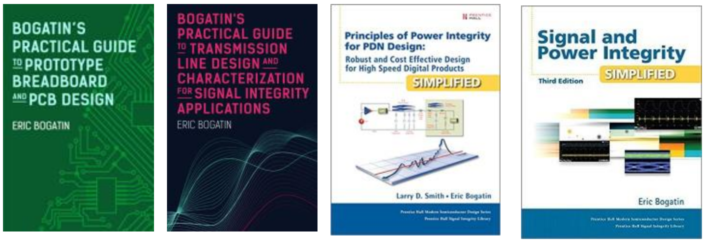
- Physics: BS MIT '76 and PhD U of A Tucson, '80
- Senior management and engineering positions at Bell Labs, Raychem, Sun Micro, Ansys, Interconnect Devices Inc
- Started Bogatin Enterprises in 1992, created the Signal Integrity Academy, acquired by LeCroy in 2011. Teledyne LeCroy Fellow to present
- Full time Prof, ECEE dept University of Colorado, Boulder, since 2021, teaching signal integrity, PCB design, Capstone Senior Design Lab
- Author: 15 books, including popular textbooks and science fiction novels, monthly columns

Other Resources



Series of free recorded webinars listed on www.beTheSignal.com

https://podcasts.signalintegrityjournal.com

Special offer for all attendees:
Sign up for complimentary 3-month subscription to the 200 hours of video training on the Signal Integrity Academy
https://www.bethesignal.com/bogatin/3monthsubscription.php Use promo code: WEB23

Agenda

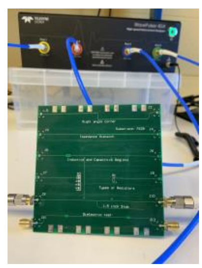
- About the CU- HSDE Group
- Four examples of cross talk with a common root cause and solution
  1. Ground bounce with and without continuous return plane
  2. Rail collapse in the power distribution
  3. Switching noise when signals cross cavities
  4. Near field emissions as a “hint” of far field emissions

Major Research Programs of the HSDE Group

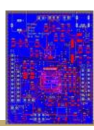
- <u>Low-Cost</u> Hands-On **Demonstrations** of SI/PI/EMI Best Design, Simulation, Measurement, Analysis Practices and Pathological Examples (primary audience is course content)
- <u>Low-Cost</u> SI/PI/EMI **Technology Solutions** (primary audience is engineers)
- Best practices for improving **Measurement-Simulation Correlation** of Circuits and Interconnects from 1 Hz to 40 GHz
- <u>Low-Cost</u>, High-Performance **Software Defined Instruments**
- <u>Low-Cost</u> **Rapid Prototyping** Best Practices

A New PMP in HSDE

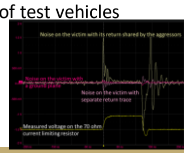
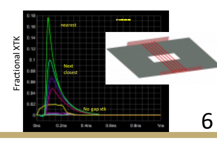
- Developing a 2-year Professional Masters Program (PMP) in High-Speed Digital Engineering
- Launching Spring 2023: https://www.colorado.edu/ecee/academics/graduate-programs/professional-masters/high-speed-digital-engineering-coming-soon
  - Signal integrity
  - Power integrity
  - EMI/EMC engineering



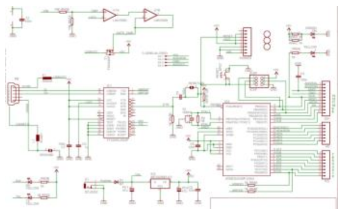
- Focusing on practical training:
  - ✓ Professional development: teamwork, communications
  - ✓ Fundamental SI/PI/EMC-EMI engineering principles
  - ✓ Best **Design**, **Simulation**, **Measurement**, and **Analysis** Practices
  - ✓ Leverage commercial simulation, measurement tools
  - ✓ Hands-on projects with design, fabrication, measurement, and simulation of test vehicles

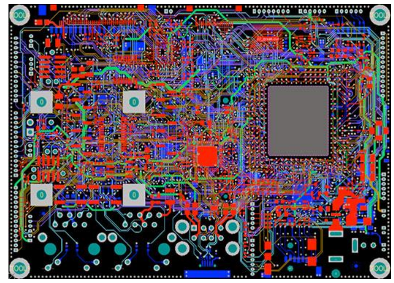


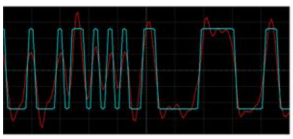
Once Connectivity is Established, the ONLY Thing Interconnects Will Do is Screw up the Signals: Add Noise



Interconnects are transparent in the schematic. They come alive in the layout



Input signals + Maxwell's Equations + Boundary conditions = Output signals

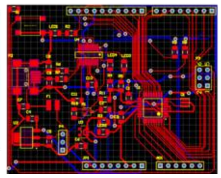


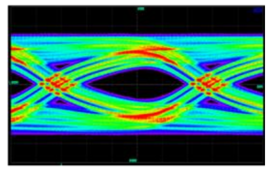
$$\Psi = \oint_S \mathbf{D}\cdot d\mathbf{S} = \iiint_V \rho_v \, dV \quad (\nabla\cdot\mathbf{D} = \rho)$$

$$\oint_C \mathbf{E}\cdot d\mathbf{l} = -\frac{d}{dt}\iint_S \mathbf{B}\cdot d\mathbf{S} \quad \left(\nabla\times\mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}\right)$$

$$\oint_S \mathbf{B}\cdot d\mathbf{S} = 0 \quad (\nabla\cdot\mathbf{B} = 0)$$

$$\frac{1}{\mu_0\varepsilon_0}\oint_C \mathbf{B}\cdot d\mathbf{l} = \frac{1}{\varepsilon_0}\iint_S \mathbf{J}\cdot d\mathbf{S} + \frac{d}{dt}\iint_S \mathbf{E}\cdot d\mathbf{S}$$





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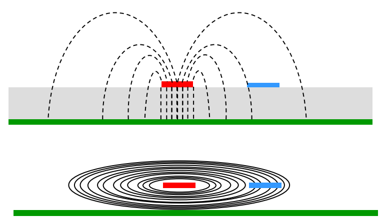
Cross Talk in Uniform Transmission Lines is Due to Fringe E and B Fields

- Induced cross talk noise:
  - ✓ Changing mutual electric field (approximate by C)
  - ✓ Changing mutual magnetic fields (approximate by L)
- Two general ways of reducing mutual field lines
  - ✓ Move the traces farther apart
  - ✓ Bring return plane closer to the signal lines
- With wide return plane, which is larger: coupled C or coupled L noise?



- Pathological cross talk: When the return plane is not wide and continuous, cross talk dramatically increases

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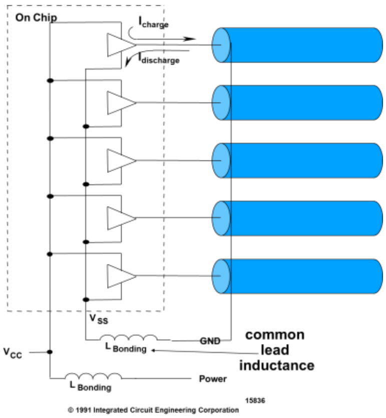
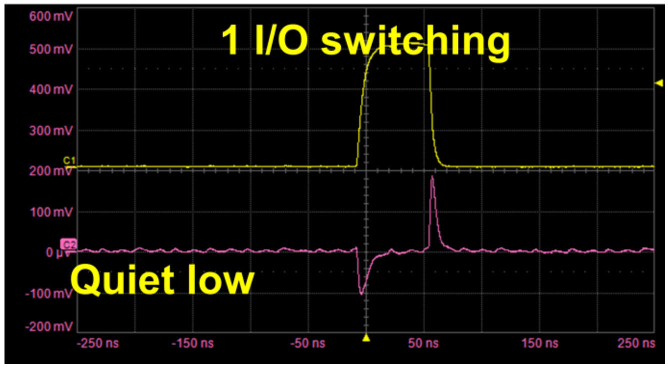
Pathological Cross Talk: Much Larger Than With Uniform Planes

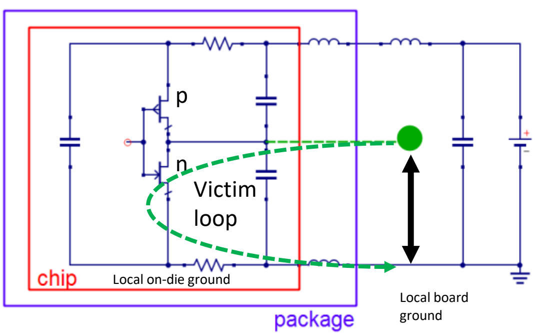
Ground Bounce





Very Useful Technique: Quiet LOW as Sense Line

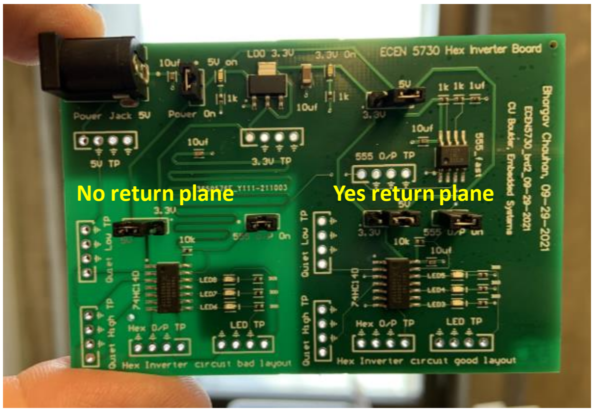
I/O pin pegged LOW

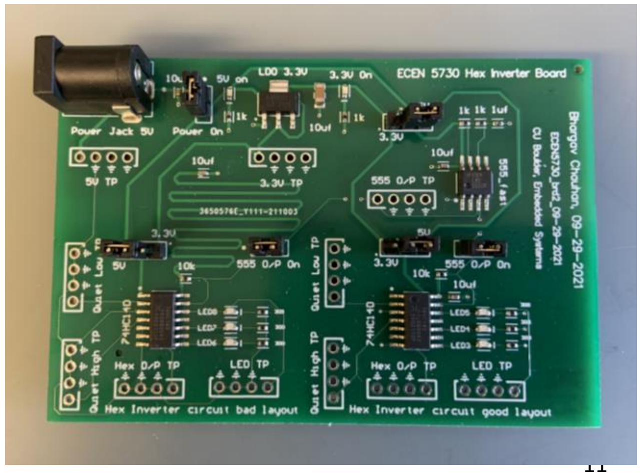


Measured voltage = total cross talk on victim line:
common lead inductance + other mutual inductance

Example 1: ground bounce with and without a continuous return plane

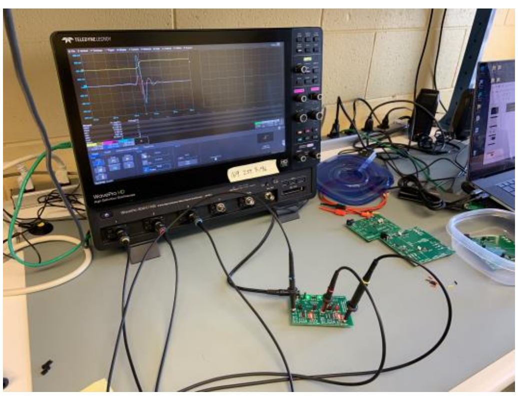
Circuit is hex inverter with 3 I/O switching 30 mA each through LEDs

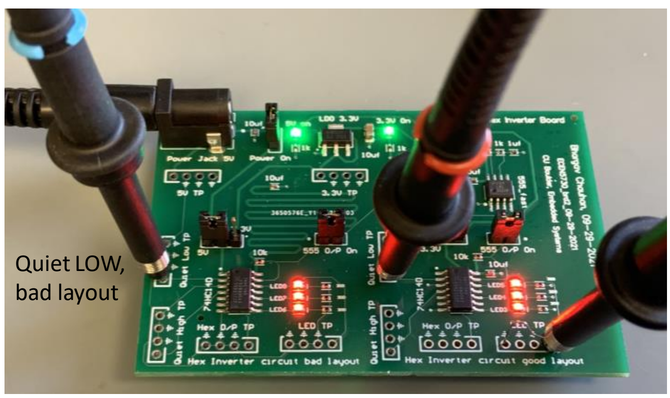




Measure a quiet LOW on good layout and bad layout sides

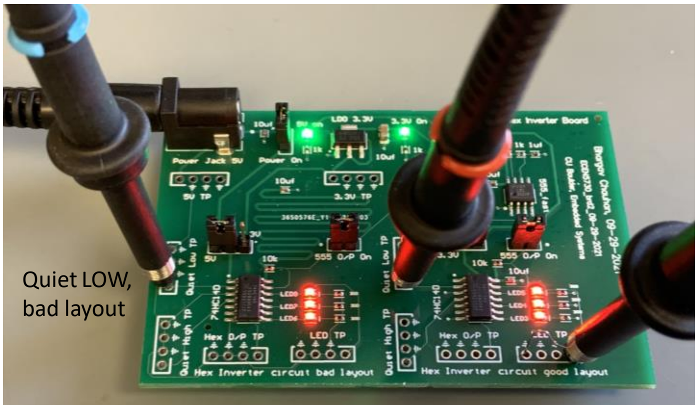
Measurement Set Up





Quiet LOW, good layout   Scope trigger

Example 1: ground bounce with and without a continuous return plane



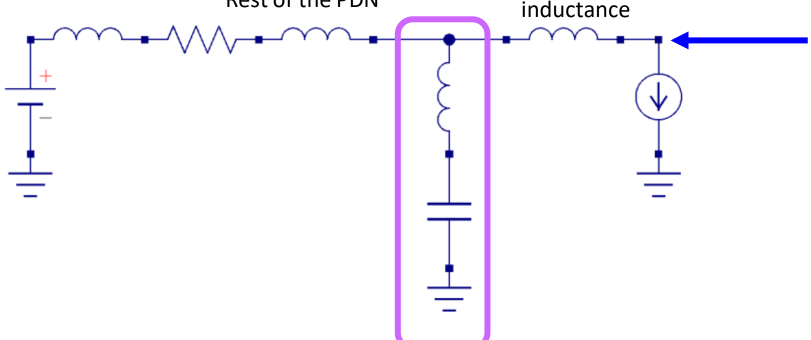
Quiet LOW, good layout

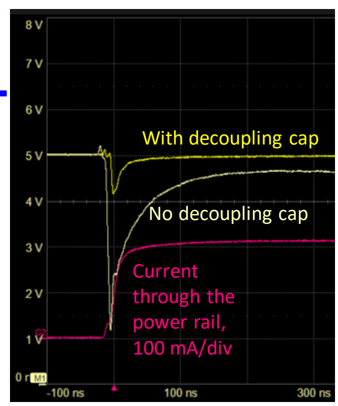
Scope trigger

3 I/O switching 30 mA each:
2 nsec rise time, 5 V signal swing
Bad layout is 1.3 V pk-pk switching noise
Good layout is 0.5 V pk-pk switching noise (package inductance)

Example 2: Rail Collapse in the Power Distribution

Simplified model of the PDN

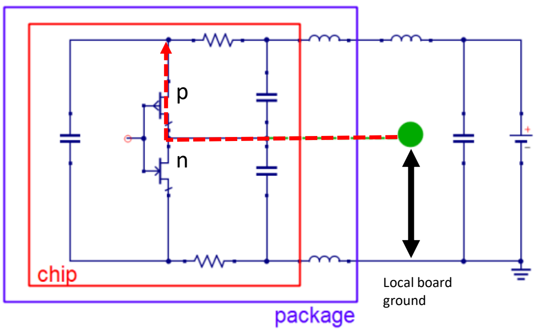




Switching noise on-die is reduced by reducing the Die-to-capacitor inductance

Very Useful Technique: Quiet HIGH as Sense Lines

I/O pin pegged HIGH



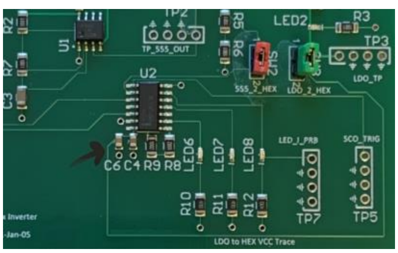
Measured voltage = voltage on die power rail relative to local brd gnd:
Vcc on die + Vss on die

Rail compression = ΔV between the Vcc and Vss on-die rails

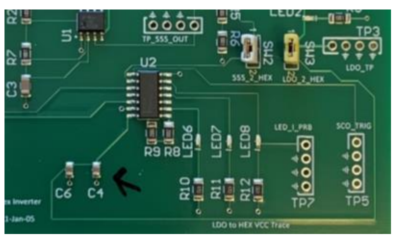
Example 2: PDN noise with different decoupling capacitor location

Identical boards. Just differ by placement of the 2 decoupling capacitors for the hex inverter

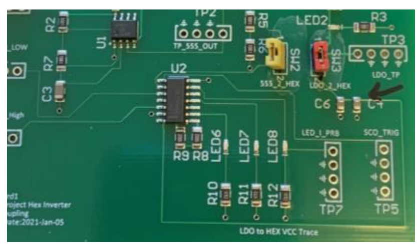
Capacitors close to IC



Capacitors far from IC



Capacitors even farther from IC

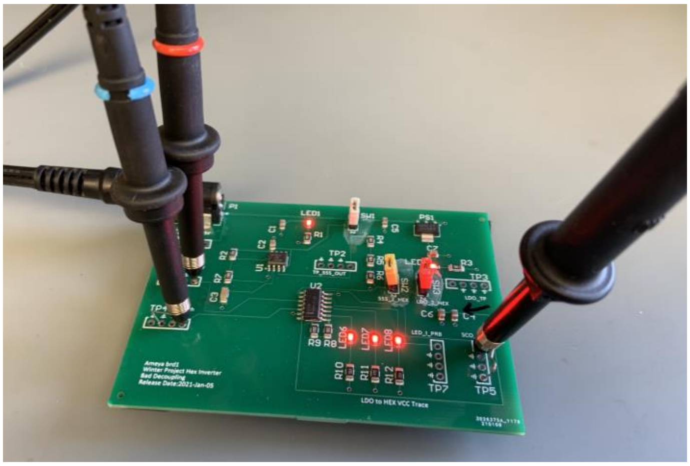


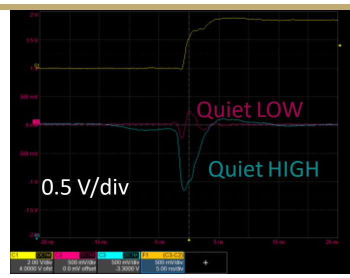
3.3 v power rail
2 nsec rise time
~ 90 mA switching current

Trace loop inductance per length ~ 20 nH/inch

Measured Quiet LOW, HIGH, Rail Compression

Rail compression = ΔV between the Vcc and Vss on-die rails





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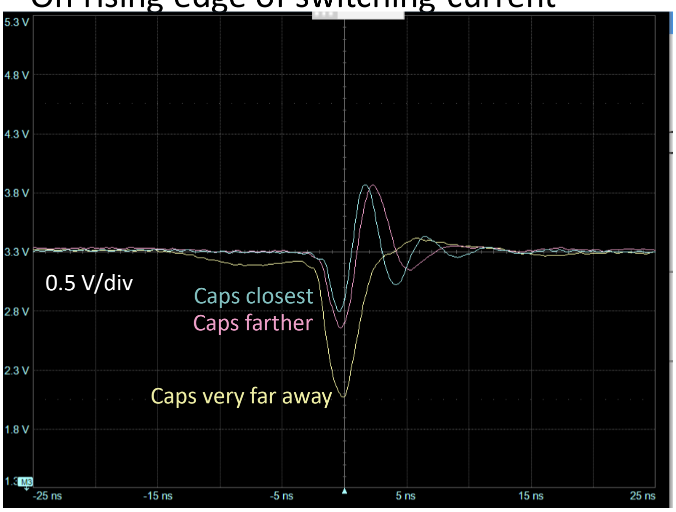
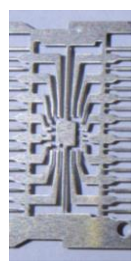
1.2 V rail compression droop on a 3.3 V raill

Rail Compression with Capacitor Placement

On rising edge of switching current



Still 0.5 V droop rail compression with caps closest- limited by the lead frame package design



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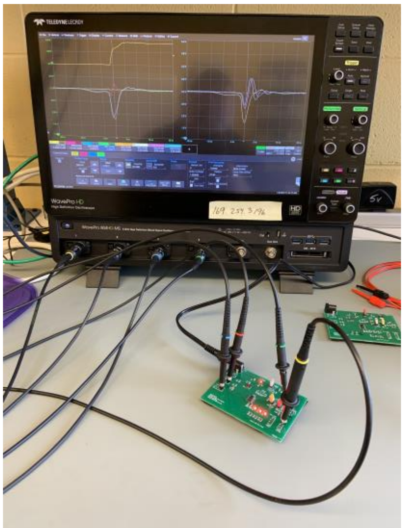
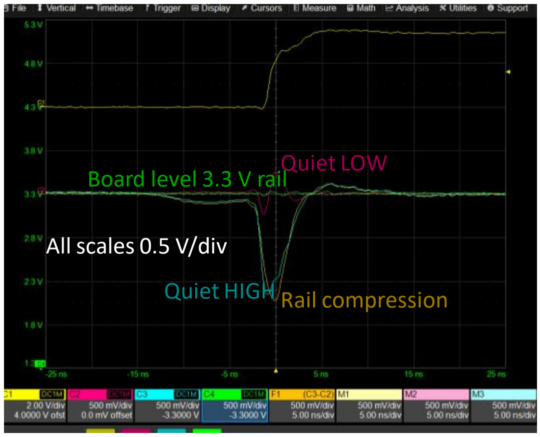
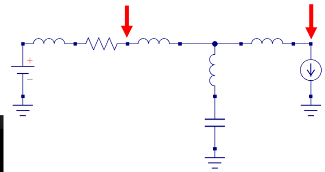
Why Don't You Typically See This Noise Level?



Using 4-probes

4[th] probe measures the on-board 3.3 V power rail





Vcc = 3.3 V

On-die rail compression = 1.2 V

On-board rail droop < 0.05 V

Example 3: Stack-Up Options for 4-Layer Boards

S/P/G
S/P/G
S/P/G
S/P/G

All signal layers

S/P
G
S/P-X
S/P-Y

3 signal layers

Which is better?

S/P
G
G
S/P/G

Ground in the middle

G
S/P
S/P
G

Ground in the outside

S/P
G
S/P
G

Ground Alternating

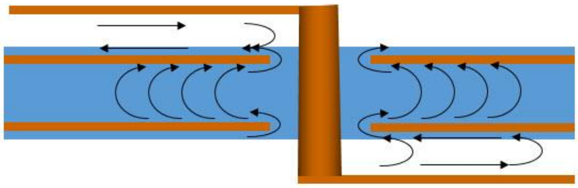
S
G
P
S

Power and ground planes

Just because a previous design used a specific feature and the product "worked" does not mean it was the best solution.

The Problem of Via-to-Via Cross Talk

When the two planes are different voltages



Power and ground planes

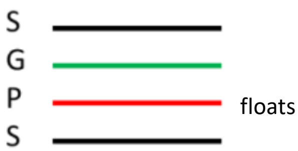
When multiple signals change return planes, the return current flows through the impedance of the power-gnd plane cavity

When current flows through an impedance, you get a voltage: seen by victim vias: cross talk

Reduce the via-to-via cross talk by reducing the impedance of the cavity- add shorting vias between the two planes (only if they are the same voltage, ie, gnd)

A DC blocking capacitor makes a poor shorting via (L ~ 2-10x a shorting via)

Example 3: Via to Via Cross Talk in a 4-layer board



Power and ground planes

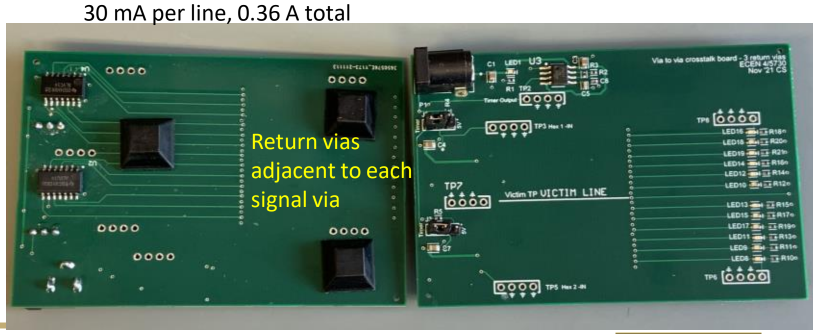
Layer 3 (power) floats- no connections at all

Twelve signals routed from layer 4 to layer 1

Twelve signals switch simultaneously

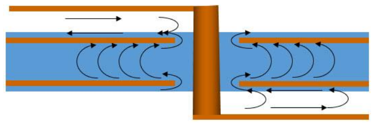
Rise time ~ 1 nsec

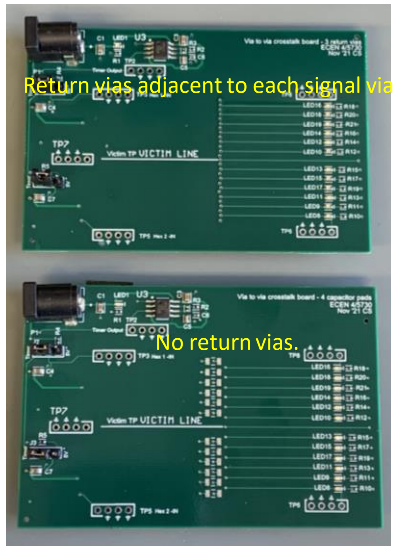
30 mA per line, 0.36 A total



Two Identical Boards, except….

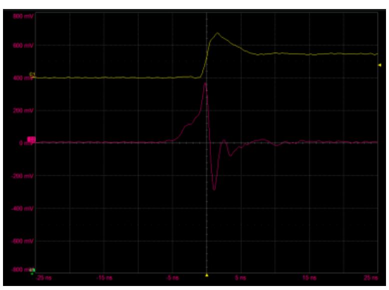
Power and ground planes





- 2 identical boards
- Layer 3 (power) floats- no connections at all
- Twelve signals routed from layer 4 to layer 1
- Twelve signals switch simultaneously
- Rise time ~ 1 nsec
- 30 mA per line, 0.36 A total

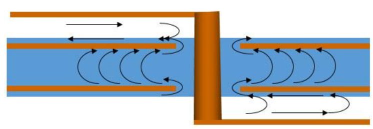
Measured Noise on Victim Trace, no Return Vias



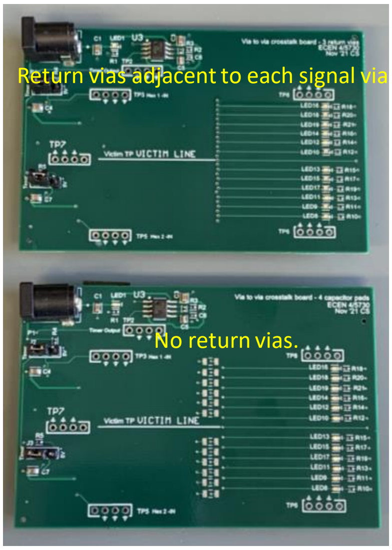
5 V signal, 360 mA switching in 1 nsec

Noise on victim trace = 600 mV pk-pk

Edge is 6 inches long, board is 3 long. Noise would be seen everywhere on the board the same

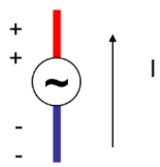


Example 3: Via to Via Cross Talk in a 4-layer board



Select two inner layers as both ground so that you have the option of adding shorting vias adjacent to each signal via that transitions

Example 4: Near Field Emissions as a "Hint" of Far Field Emissions



Isolated dipole

Multipole expansion of the radiated field

$$E(r) = k_1 \frac{1}{r} + \boxed{k_2 \frac{1}{r^2} + k_3 \frac{1}{r^3} + k_4 \frac{1}{r^4} + \cdots}$$

Far field term (dipole)

Near field terms
Higher order moments- drop off quickly with distance

Near field for 100 MHz < 10 ft

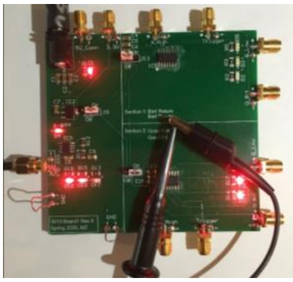
Near field measurements measure emissions from multipole moments, not just dipole terms.

Noise measured in the near field may not appear in the far field

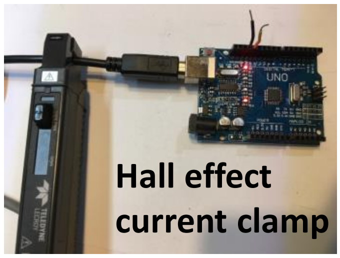
But, far field radiation will always appear in near field

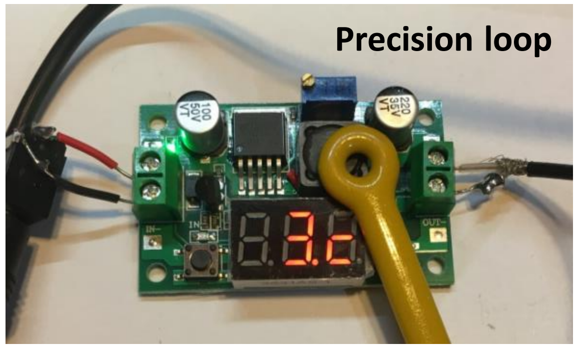
And, near field measurements do not require a chamber

Simple Methods of Measuring Near Field Emissions (inductive cross talk)



10x probe loop





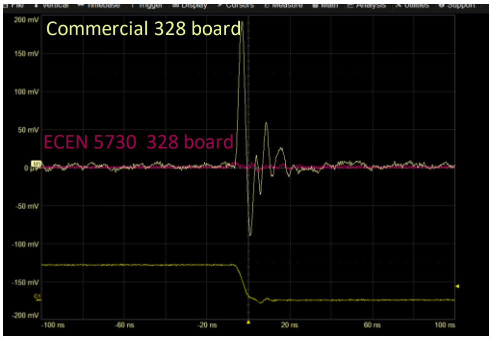
Two Identical Circuits, Very Different Layout

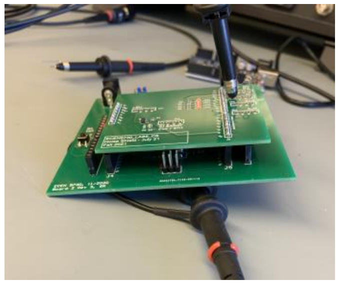
Atmega 328 micro controller boards

Commercial board has copper pour on top and bottom layers: discontinuous return plane (gaps in return path)

ECEN 5730 board has continuous return with short cross unders

Example 4: Near Field Emissions





Continuous return plane dramatically reduces near field emissions

Deciding Between Alternative Design Choices

Situation Analysis:

- ✓ Most design decisions are a balance of tradeoffs: noise, cost, risk, schedule, supply chain, corporate history, …
- ✓ Once connectivity is established, interconnect performance is about reducing noise.
- ✓ If you don't measure the noise, how do you know how much there is?
- ✓ If noise is below an acceptable level, your design may have "worked" ***in spite of*** your design choices, not ***because*** of them.
- ✓ The specific test vectors you used may not have exercised the worst case, which a customer is guaranteed to find.

Recommended Guidelines:

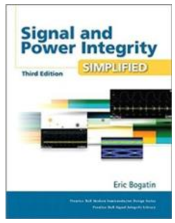
- ✓ Understand design choices based on fundamental principles, and by "Putting in the Numbers"
- ✓ Explore design space with virtual prototypes or well characterized real prototypes
- ✓ If a design decision reduces noise and has little impact on other costs, it should become a habit

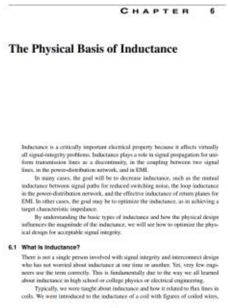
Most Important Take-Away

Avoid pathological cross talk by controlling inductance:

- ✓Loop inductance between Vcc pin and nearest decoupling capacitor
- ✓Common shared return path inductance
- ✓Higher total inductance return paths in other than wide, continuous return paths
- ✓Mutual inductance between signal-return path pairs

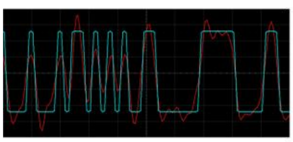
If you want to be a better board designer, understand the physical basis of inductance





Ingredients for Success

Input signals + Maxwell's Equations + Boundary conditions = Output signals

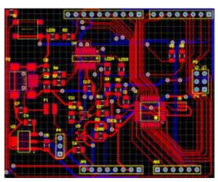


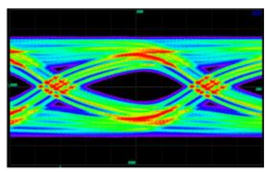
$$\Psi = \oint_S \mathbf{D}\cdot d\mathbf{S} = \iiint_V \rho_v\, dV \quad (\nabla\cdot\mathbf{D} = \rho)$$

$$\oint_C \mathbf{E}\cdot d\mathbf{l} = -\frac{d}{dt}\iint_S \mathbf{B}\cdot d\mathbf{S} \quad \left(\nabla\times\mathbf{E} = -\frac{\partial\mathbf{B}}{\partial t}\right)$$

$$\oint_S \mathbf{B}\cdot d\mathbf{S} = 0 \quad (\nabla\cdot\mathbf{B} = 0)$$

$$\frac{1}{\mu_0\varepsilon_0}\oint_C \mathbf{B}\cdot d\mathbf{l} = \frac{1}{\varepsilon_0}\iint_S \mathbf{J}\cdot d\mathbf{S} + \frac{d}{dt}\iint_S \mathbf{E}\cdot d\mathbf{S}$$



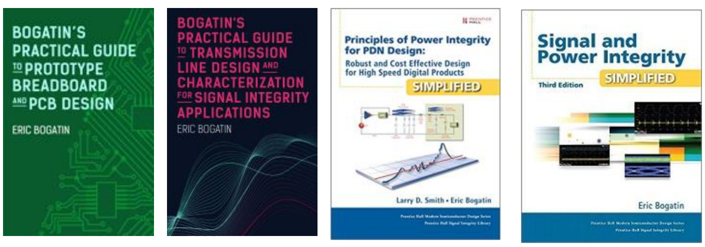


- Requires skill in:
  - ✓The fundamental principles
  - ✓Applied Maxwell's Equations
  - ✓Best Design Practices
  - ✓Best Simulation Practices
  - ✓Best Measurement Practices

Thanks to the Generous Support From

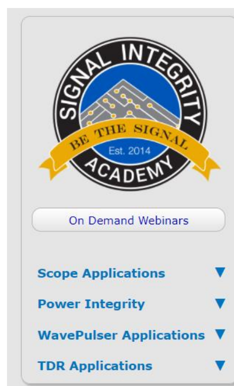
- Curriculum development support from:
  - ✓ Ansys
  - ✓ Siemen's Mentor Graphics
  - ✓ Keysight
- Teledyne LeCroy: $500k of high-speed measurement equipment:
  - ✓ 8 GHz scope
  - ✓ 30 GHz VNA
  - ✓ 35 psec rise time diff TDR
  - ✓ Other scopes, probes
- Rohde and Schwarz
- Wild River Technologies
- Samtec
- AVX
- GE Health Care
- Qualcomm

Other Resources



https://podcasts.signalintegrityjournal.com

Series of free recorded webinars listed on www.beTheSignal.com



Special offer for all attendees:
Sign up for complimentary 3-month subscription to the 200 hours of video training on the Signal Integrity Academy
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Thank you!

Questions?

University of Colorado, Boulder, ECEE High Speed Digital Engineering Group

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