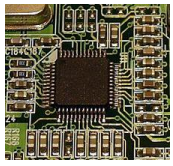
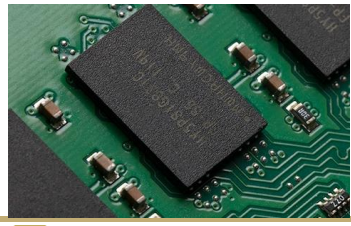


Decoupling Capacitors and PCB Layout: What is Really Important?

Prof Eric Bogatin

Eric.Bogatin@colorado.edu



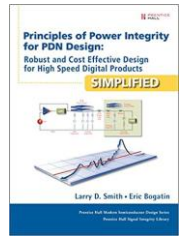
Spring 2023

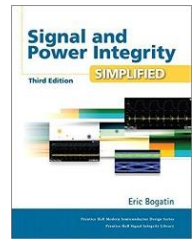
About the Eric

Eric Bogatin
Prof, University of Colorado, Boulder
Fellow: Teledyne LeCroy
Technical Editor, Signal Integrity Journal

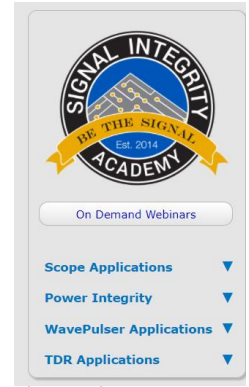
- Physics: BS MIT '76 and PhD U of A Tucson, '80
- Senior management and engineering positions at Bell Labs, Raychem, Sun Micro, Ansys, Interconnect Devices Inc
- Started Bogatin Enterprises in 1992, created the Signal Integrity Academy, acquired by LeCroy in 2011. Teledyne LeCroy Fellow
- Full time Prof, ECEE dept University of Colorado, Boulder, since 2021, teaching signal integrity, PCB design, Capstone Senior Design Lab
- Author: 15 books, including popular textbooks and science fiction novels, monthly columns

Other Resources





Series of free recorded webinars listed on www.beTheSignal.com



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3

Major Research Programs of the HSDE Group

- Low-Cost Hands-On **Demonstrations** of SI/PI/EMI Best Design, Simulation, Measurement, Analysis Practices and Pathological Examples (primary audience is course content)
- Low-Cost SI/PI/EMI **Technology Solutions** (primary audience is engineer)
- Improving **Measurement-Simulation Correlation** of Circuits and Interconnects from 1 Hz to 40 GHz
- Low-Cost **Software Defined Instruments**

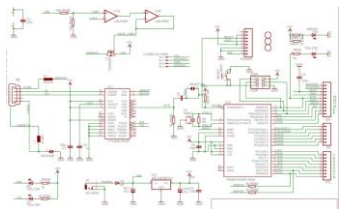
4

Agenda

- Challenges in PDN design
- One example: rail collapse for I/O switching
- An homage to Bob Pease
- So what? good and not so good PCB layout strategies
- Legacy Code
- Final recommendations

Design is First About Connectivity

A schematic identifies:
- BOM
- Functionality
- Connectivity
- Wires are transparent- no R, no delay

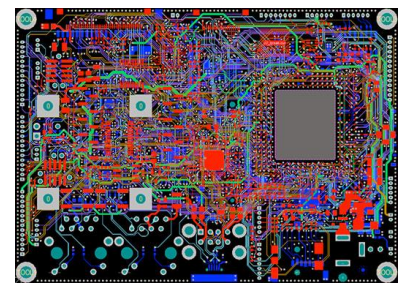


The interconnects live in the wires and the white space of the schematic

If the interconnects are transparent, design for performance doesn't apply. It's all about connectivity, DFM, DFR, DFT,…

…but, in almost every design, they are not transparent

A layout represents the physical design of the interconnects

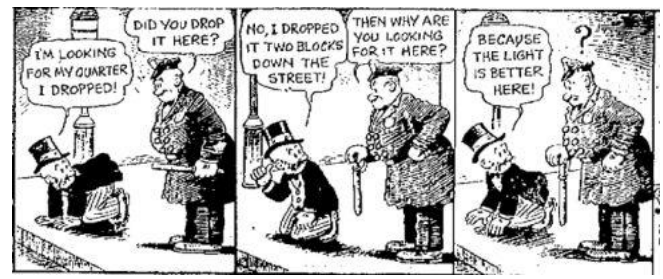


Once connectivity is correct, the only thing interconnects are going to do is screw up the performance
The goal in interconnect design is to minimize how much the interconnects screw things up

Four Hurdles in PDN Design

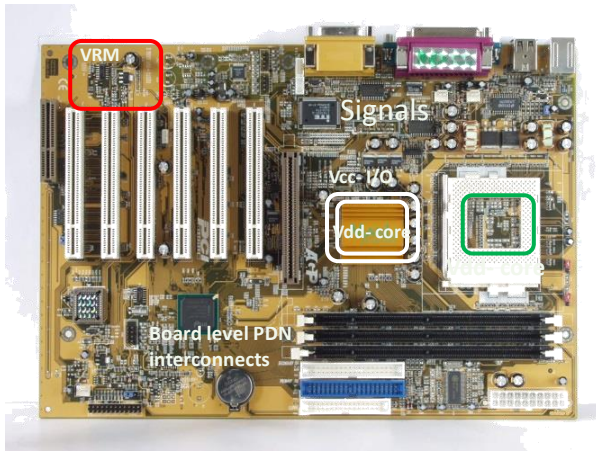
- The problem with PDN design is not 1 problem, it is 12 problems
- Identifying the root cause of each problem is hard
- There are 9 orders of magnitude between low current PDNs (1 uA) and high current PDNs (1000 A). One solution cannot apply to all
- There is a lot of “noise” and “legacy code” circulating in the industry about PDN design

Watch out for the “streetlight effect”: a common origin for PDN design guidelines



The right solution is not always where it’s easy to find

Why PDN Design is so Confusing: It's not just 1 problem and root cause, it's 12



- Self aggression noise
  - From VRM on VRM
  - **From Vcc on Vcc (not much on-die capacitance)**
  - From Vdd on Vdd (a lot of on-die capacitance)
  - From signals on signals (discontinuities)
- "Pollution" of the board/pkg interconnects
  - From VRM
  - From I/O
  - From core
  - From signals
- Mutual aggressors: cross talk coupling from the PDN
  - To VRM
  - To I/O
  - To core
  - To signals

Best Design Practices Depend on Which PDN Problem You Are Trying to Solve

Agenda

- Challenges in PDN design
- One example: rail collapse for I/O switching
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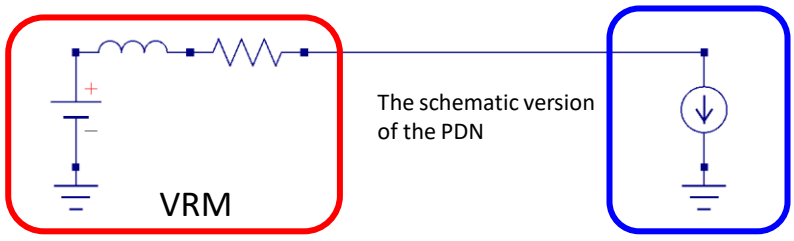
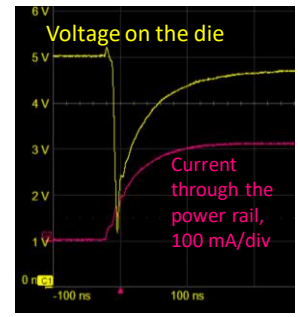
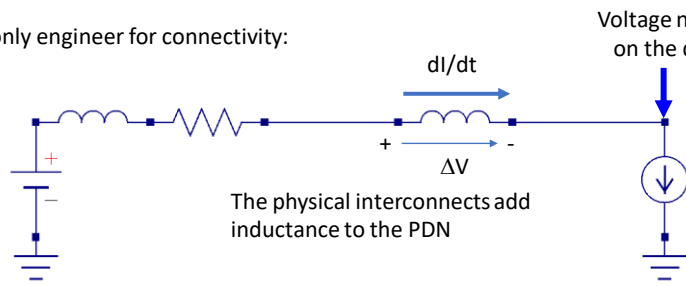
The Origin of I/O Switching Noise on the Power Rail



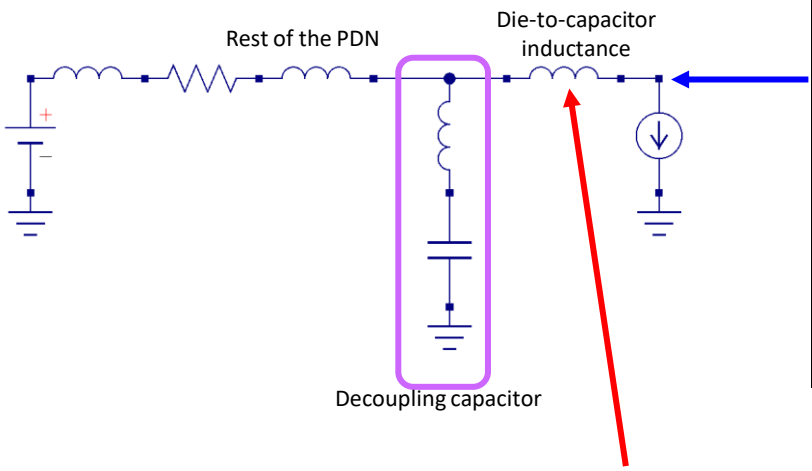


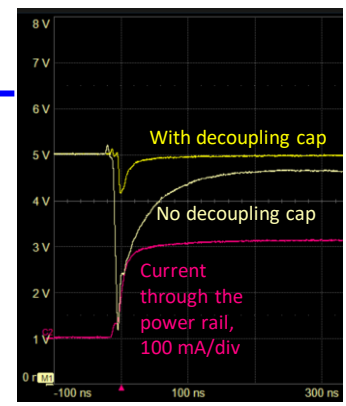
If we only engineer for connectivity:



Impact is dI/dt voltage noise on the die power rail (switching noise)

Reduce Switching Noise by adding Decoupling Capacitors "Decouples" the IC from the Rest of the PDN Inductance





Switching noise on-die is reduced by reducing the Die-to-capacitor inductance

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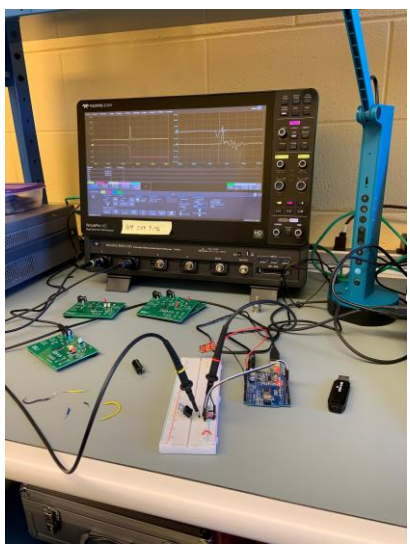
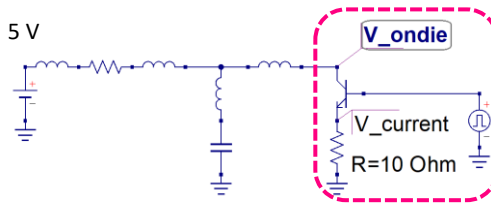
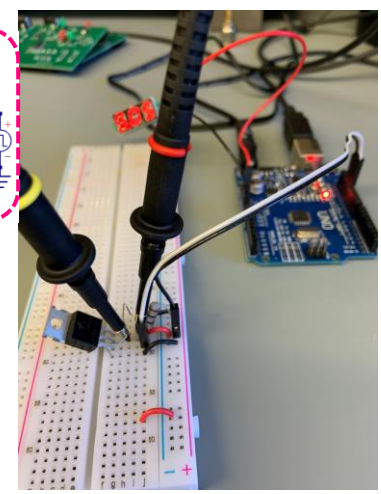
An Homage to Bob Pease, "My simulation language is solder"





Slammer circuit



Arduino drives 5% duty cycle pulses, ~ 10 nsec rise time

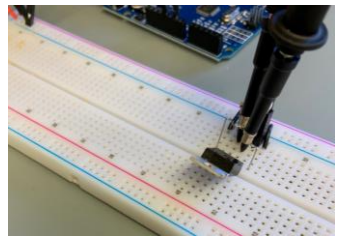
TIP41C transistor turns on in ~30 nsec

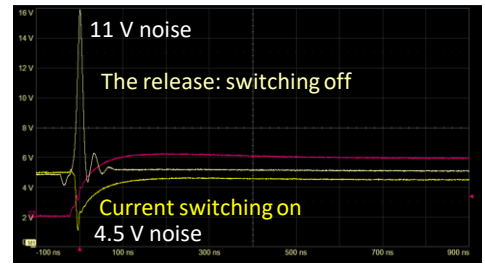
Scope measures voltage across 10 ohm resistor

Scope measures the voltage on collector (on die)

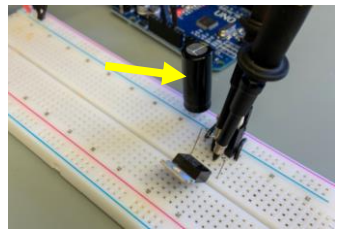
The Origin of I/O Switching Noise on the Power Rail

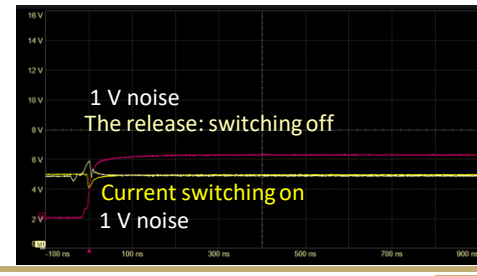
No decoupling capacitor



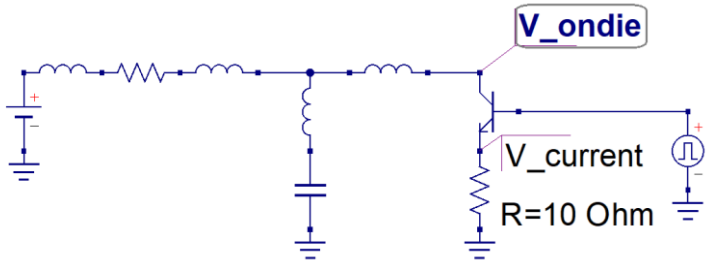


With decoupling capacitor





How Much Capacitance is Enough?

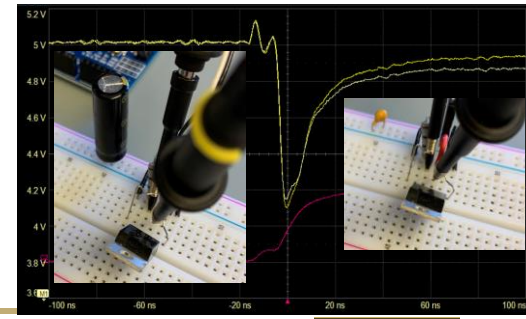


- The purpose of the capacitor is to reduce the inductance the die sees.
- How much capacitance to add?

$$C > \frac{\Delta Q}{\Delta V} = \frac{I\Delta t}{\Delta V} = \frac{0.4A \times 100n\,\sec}{0.1V} = 400nF$$

- To first order, doesn't matter how much larger the capacitor is- just that it is low inductance

Power rail noise with 1000 uF and 1 uF capacitors



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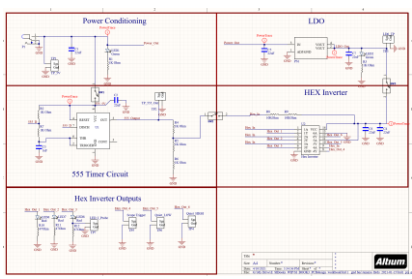
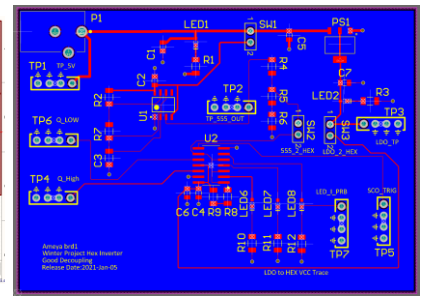
A Circuit Board Experiment

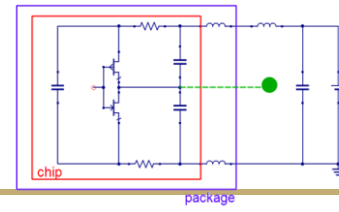
with my student Ameya Ramadurgakar





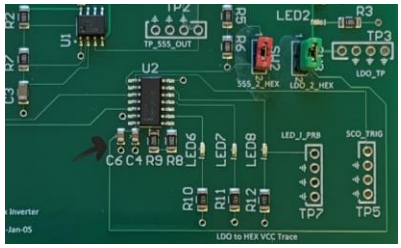
Features: 555 timer at 500 Hz

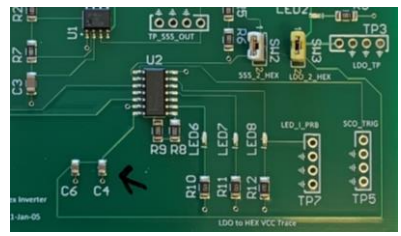
Drives inputs to Hex inverter
Outputs 1, 2, 3 drive 50 ohms and RED LED (25 mA each)
Output 4 drives trigger to scope
Output 5 is pegged low (quiet low, on die)
Output 6 is pegged HI (quiet High, on die)

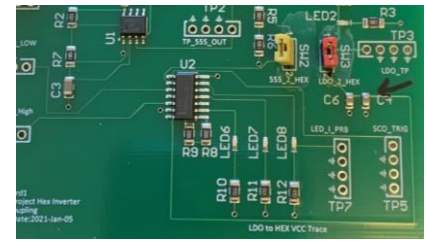


Three Identical Schematics, Different Layouts

Identical boards. Just differ by placement of the 2 decoupling capacitors for the hex inverter



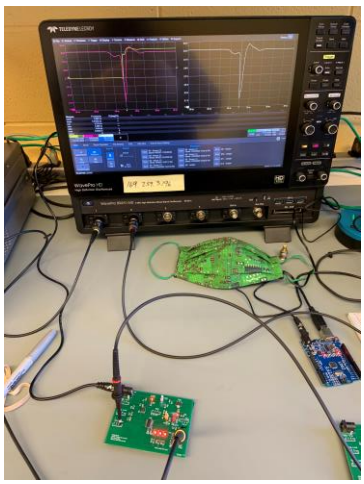


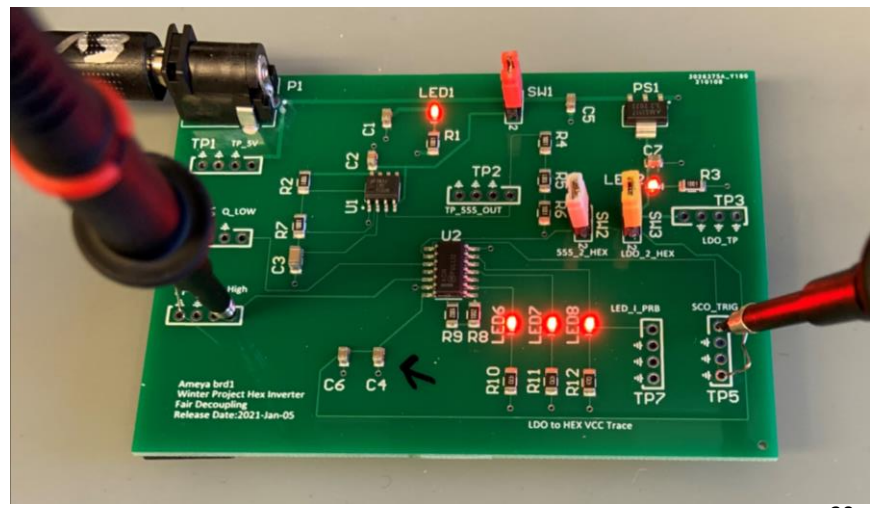


Boards designed by Ameya Ramadurgakar

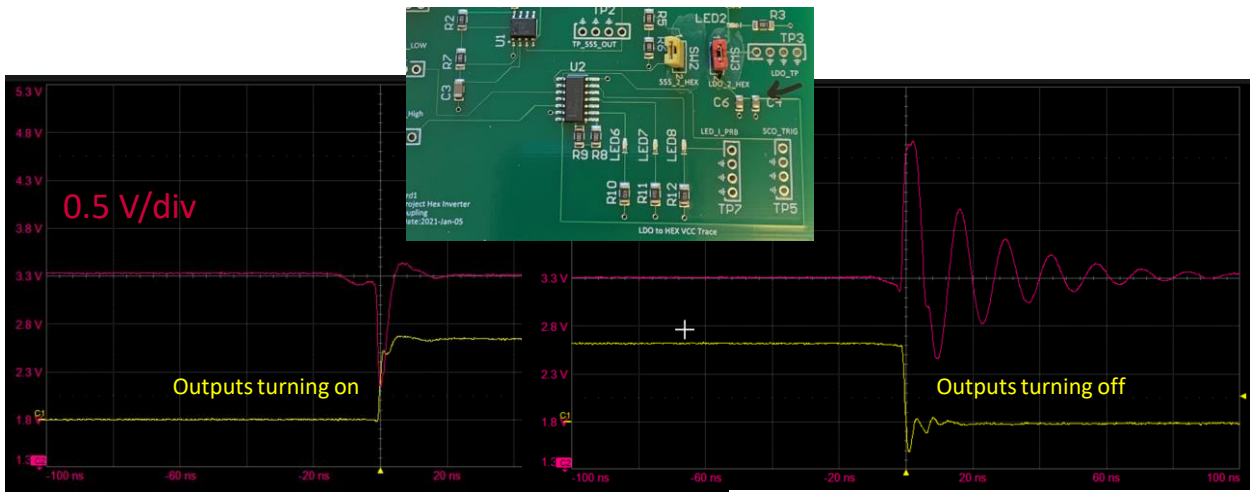
Rule #9: what do we expect?

Important Design Principle for Prototypes: Design for Test and Bring Up with 10x Probe Test Points

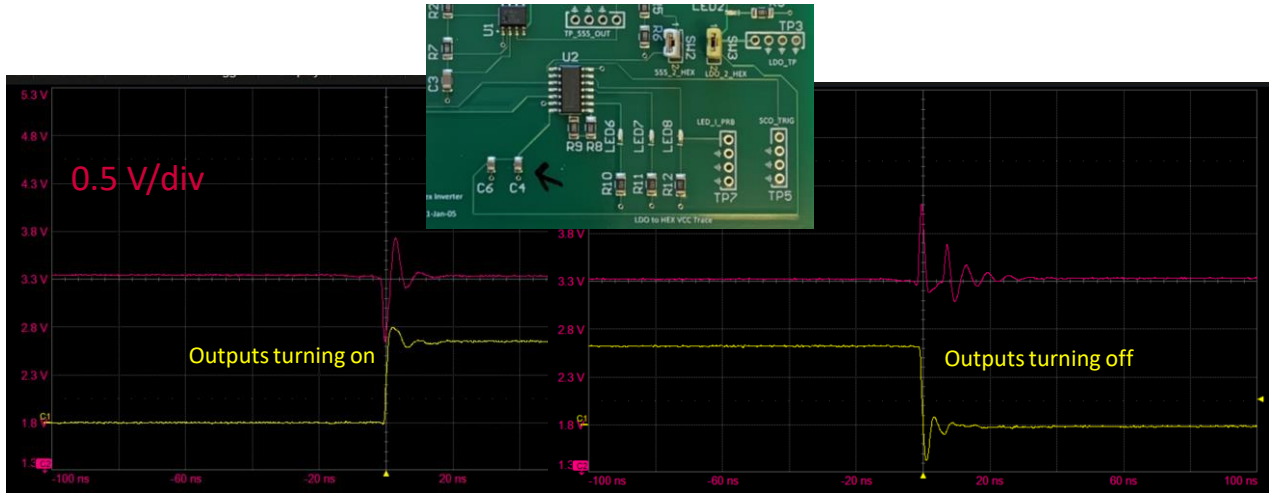




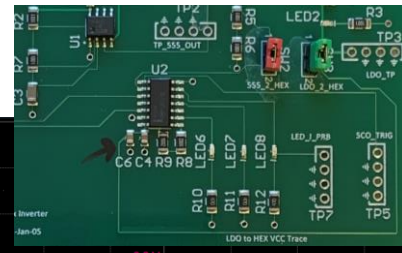
Really Bad Routing



Fair Routing

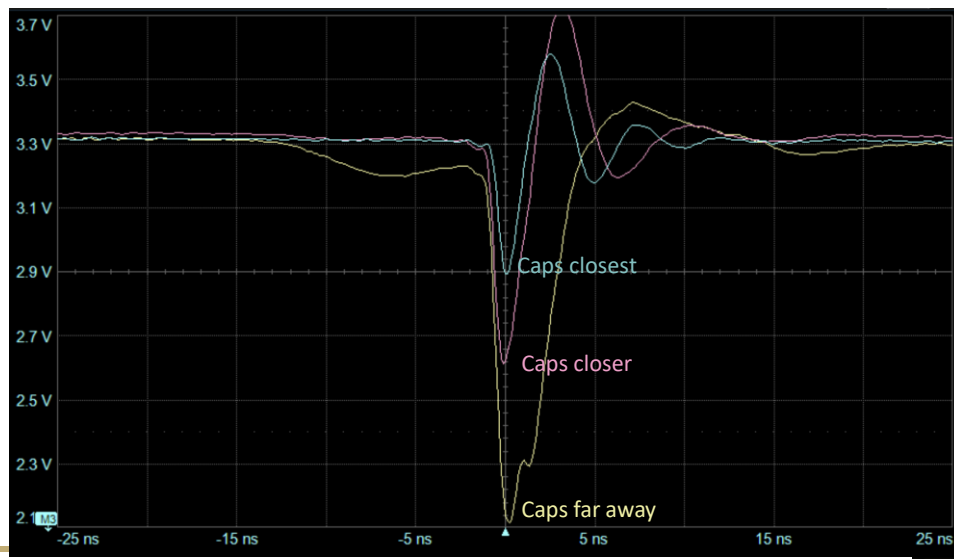


Best Routing



Limited by package lead inductance ~ 10 nH)

How the Decoupling Capacitors are Placed, Matters



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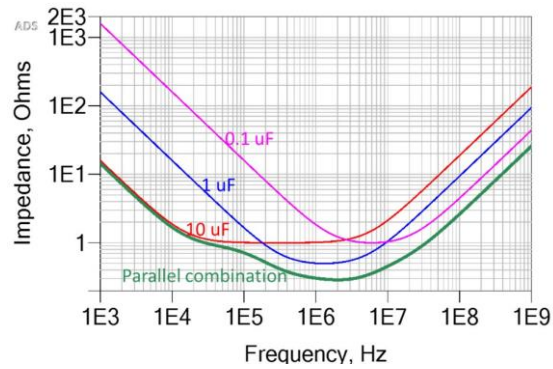
Historical Driving Force in Reducing Switching Noise: use three different value decoupling capacitors: 10 uF, 1 uF, 0.1 uF

- How to achieve low inductance?

https://www.signalintegrityjournal.com/articles/1589-the-myth-of-three-capacitor-values

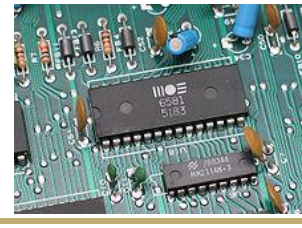
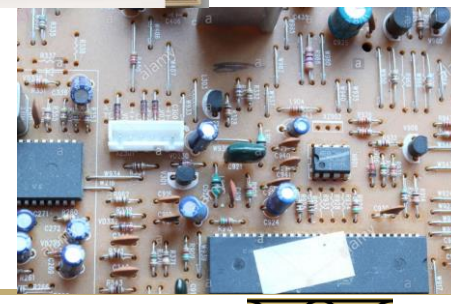


Historically:

- Smaller capacitance value capacitors were smaller physical size and lower inductance: "High frequency capacitors"
- Use small size capacitors to get low inductance. Add larger size capacitors to get more capacitance.
- The origin of the recommendation: Use three capacitors in parallel: 10 uF, 1 uF, 0.1 uF

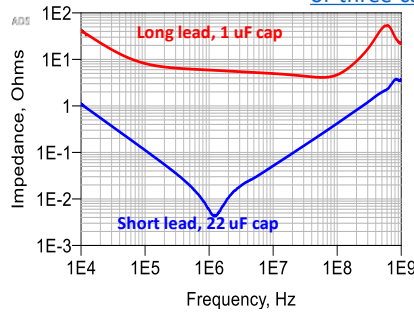
A Common Design Guideline for 50 Years



The Reality Today

https://www.signalintegrityjournal.com/articles/1589-the-myth-of-three-capacitor-values

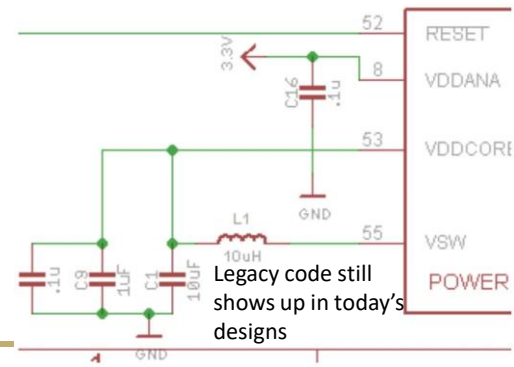


The reality:

- High frequency impedance is not about the capacitance, it is about the lead loop inductance
- A "high frequency capacitor" just has low loop inductance

Three different value capacitors is legacy code.
Use 1 capacitor, use 3 capacitors, the same value, 3 different values:

- ✓ Your design may work
- ✓ Your design may not work
- ✓ Your design may work in spite of your choice, not because of it
- ➢ Either "test in" design or do detailed analysis
- ➢ ***Low inductance is the key***



Legacy code still shows up in today's designs

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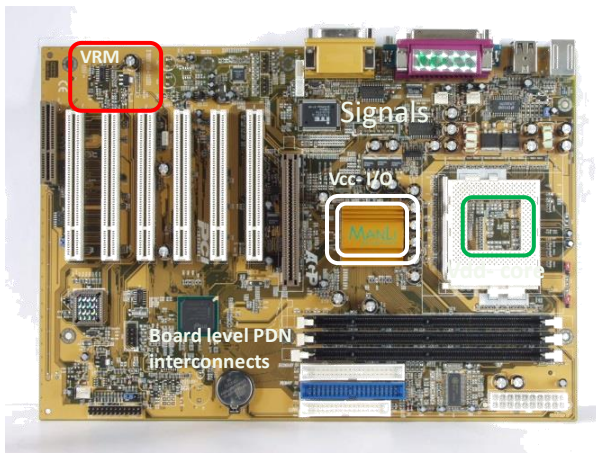

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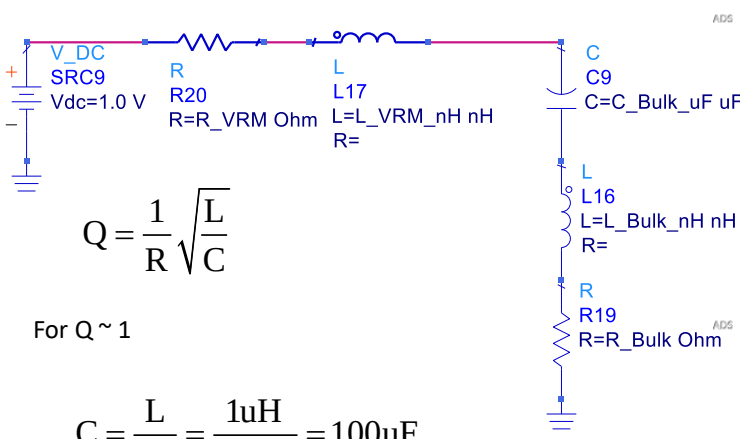
  - To signals

Best Design Practices Depend on Which PDN Problem You Are Trying to Solve

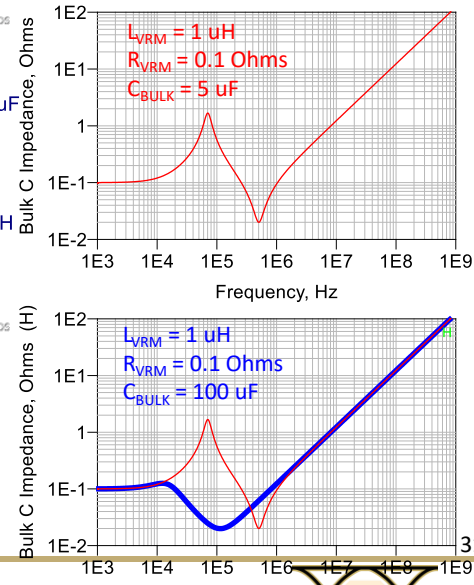
Selecting the Bulk Decoupling Capacitor is about Managing the Parallel Resonance with the VRM Inductance



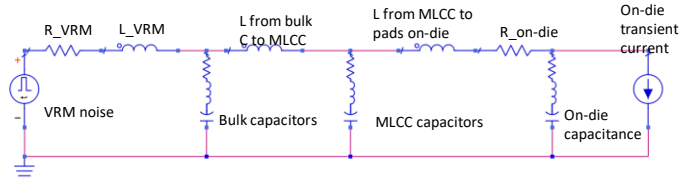
$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

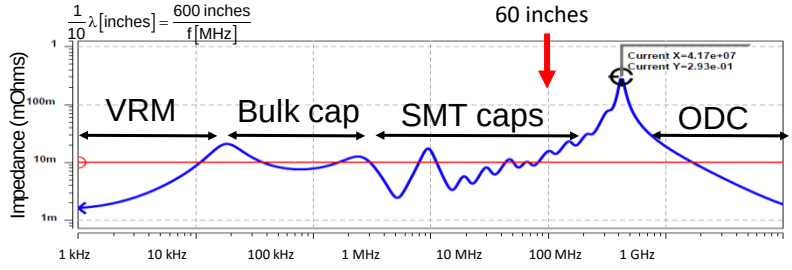
For Q ~ 1

$$C = \frac{L}{R^2} = \frac{1uH}{(0.1)^2} = 100uF$$



PDN Design for the Core Rail is Dominated by Managing the Bandini Mountain





Managing PDN impedance is about managing the peaks (parallel resonances)

Biggest parallel resonance: between the on-die capacitance and the package inductance including the ESL of the MLCC capacitors

The "Bandini Mountain"

- Steve Weir

Luck and Hope Should Not be Part of the Design Process

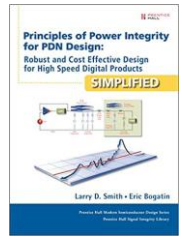
The faster you go, the less luck you seem to have

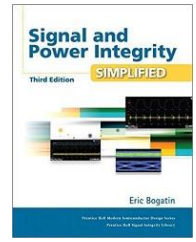
There is no substitute for applying good engineering principles

Conclusion

- Interconnects will only add noise to your product
- Reduce noise by identifying potential problems and designing them out
- Base your designs on the root cause of the potential problems
- Turn the root cause into design guidelines
- There is no substitute to good engineering principles

Other Resources





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