

# ESSENTIAL EMC PCB Design Rules

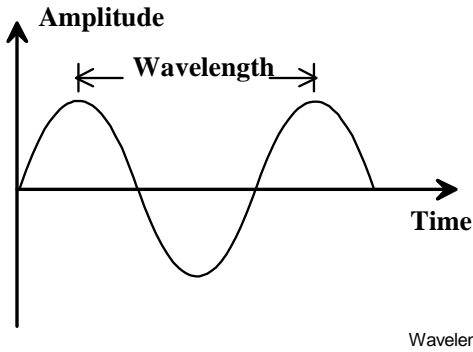
There are many design rules possible. However the following are typically the most important and a minimum requirement.

Note, this list does not address some signal integrity rules for high speed logic.

## Definitions:

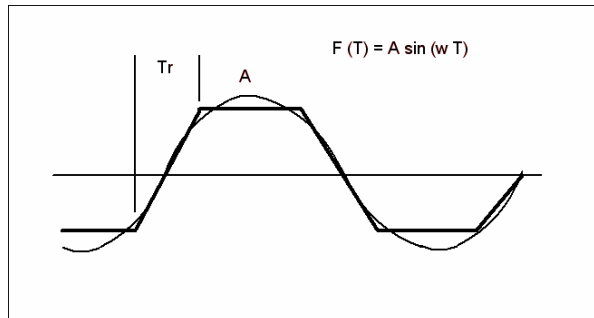
I/O = Input, Output, GP = Ground Plane, MGP = Micro Ground Plane, PCB = Printed Circuit Board

## Useful Info:



$$\lambda = \frac{300}{f(\text{MHz})}$$

## Sine Approximation of Pulse Train



$$\text{Freq} = 1 / (\pi \times \text{Tr})$$

## Square Wave Spectrum

Many EMC rules involve controlling loop area (signal-return) and current rise/fall times

## Design Guide References:

<http://www.fordemc.com/>

<http://www.cvel.clemson.edu/emc/>

Infineon AP24026

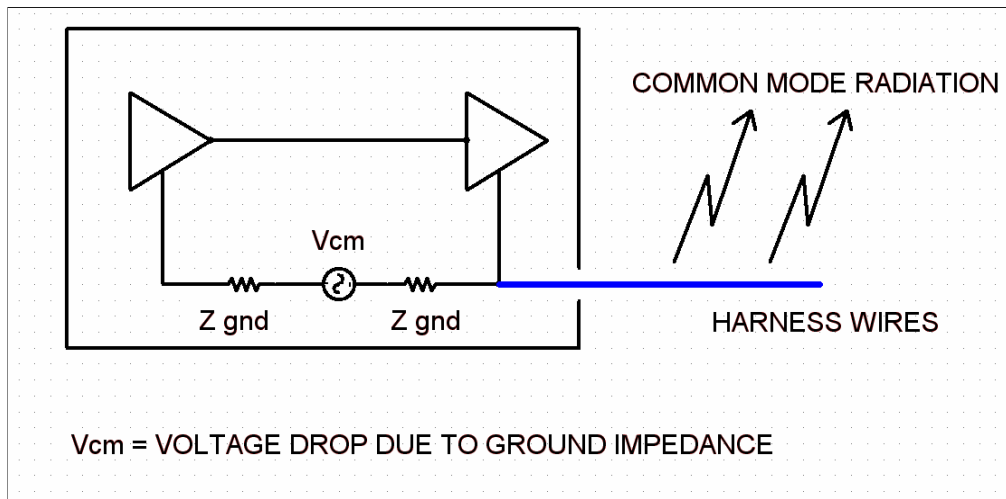
## 1. Ground Plane or Grid

A good ground structure is the most important thing for EMC. Near solid is best (e.g. on 4 layer PCB, second layer should be devoted to GP, ideally vias are the only openings). The next best alternative is a ground grid.

GP does many things - for example:

- Minimizes impedance between points on the PCB (reduces high frequency voltage drops - see fig 1.1).
  - Creates microstrips (see figure) for traces running over it (controls impedance)
  - Minimizes radiating and pickup loop area.
- a. Implemented on 2 sided PCB - horizontal ground tracks on one side and vertical ground tracks on the other. The ground tracks shall be connected with vias to form a grid like pattern. Power, signal tracks are located between ground grid tracks.
- b. About  $\frac{1}{2}$  inch grid spacing is good compromise - see table and figure below
- c. Do not have separated grounds (e.g., digital/clean, analog/dirty, 3.3V and 5V) on the board, have only one good ground plane-grid.
- d. Beware of ground fills. These ground "islands" need to be tied to the ground plane with multiple via's or many short, thick (low inductance) traces connecting them all together.

Figure 1.1



Microstrip

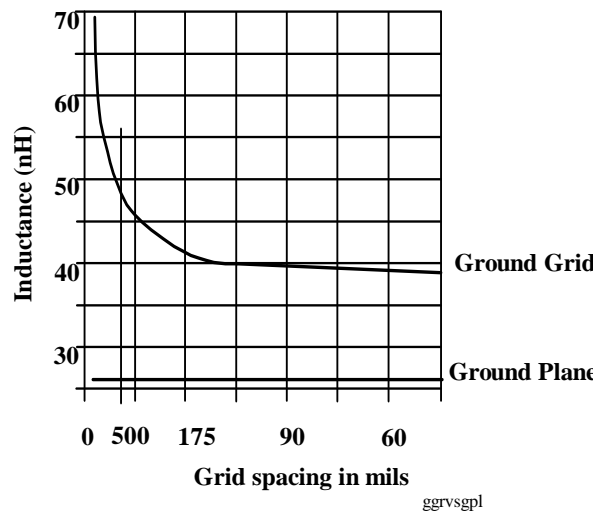


trace3pr

Table 1.1

Spacing, inches	Inductance, nh
0.9	70
0.7	55
0.35	45
0.175	42
0.12	40
0.09	39

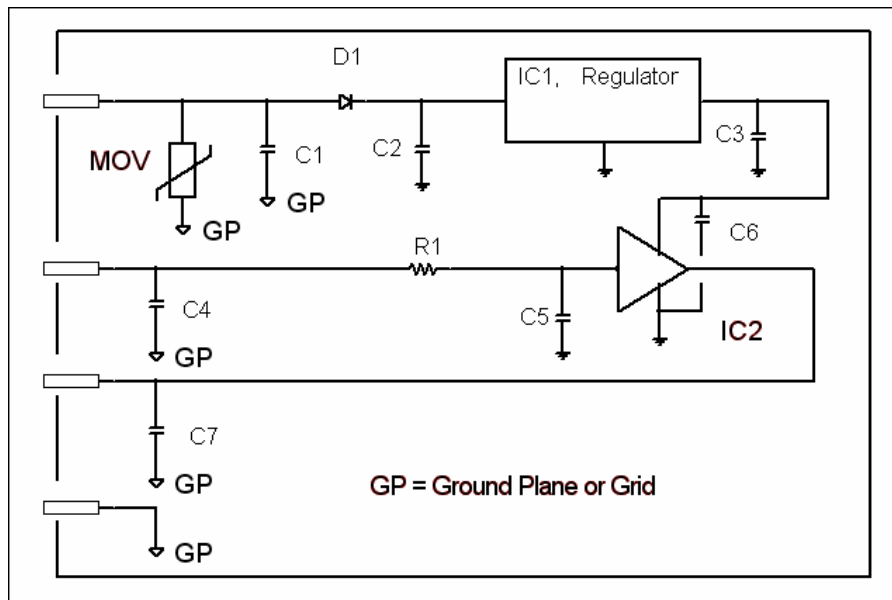
Figure 1.2



**2. I/O Filters:**

- a. All I/O shall have a capacitor near the I/O connector with little trace length (< 5mm) to ground plane-grid. This addresses radiated immunity/emissions and ESD. Trace inductance over GP = approx 20nh/inch
- b. Recommend 10 nF, 100 volt MLC capacitors on all I/O (especially safety related products). Some signals cannot tolerate such a high value - use smaller value for them (assumes that value will not distort the signal).
- c. As a minimum requirement the layout shall include pads to support adding of bypass capacitors directly at the I/O connector.

Figure 2.1

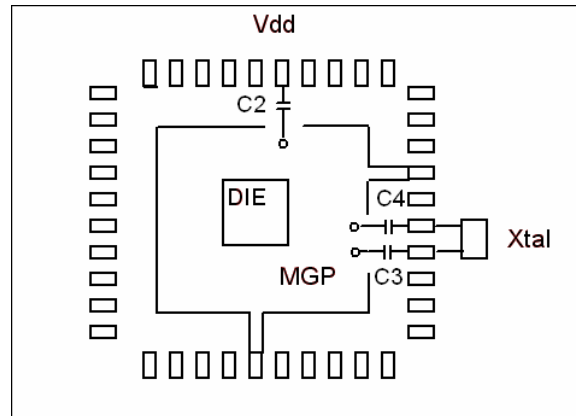


- MOV = Transient and Load Dump suppression
- C1, C4, C7 = ESD, RF filters. C1 before D1 to prevent audio rectification
- C2 = Low frequency filter (e.g. Dropouts, Alternator ripple). D1 keeps C2 charged during voltage dips/dropouts.
- C3 = Regulator filter
- C6 = Local IC decoupling

### 3. IC Decoupling Filters:

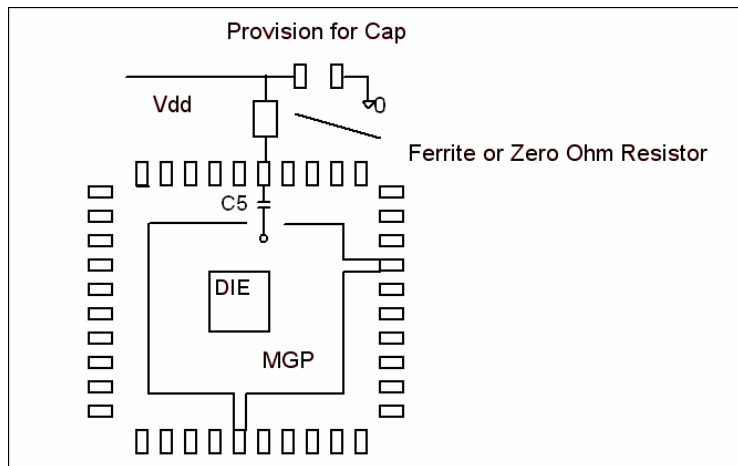
Figure 3.1 shows the recommended configuration that minimizes loop areas and track inductance.

Figure 3.1



The following configuration should be used for development during radiated emissions testing. The extra series component and capacitor may be required if the IC is very noisy. Note that the ferrite may cause current starving (too much series impedance). Verify correct IC operation at all temperatures.

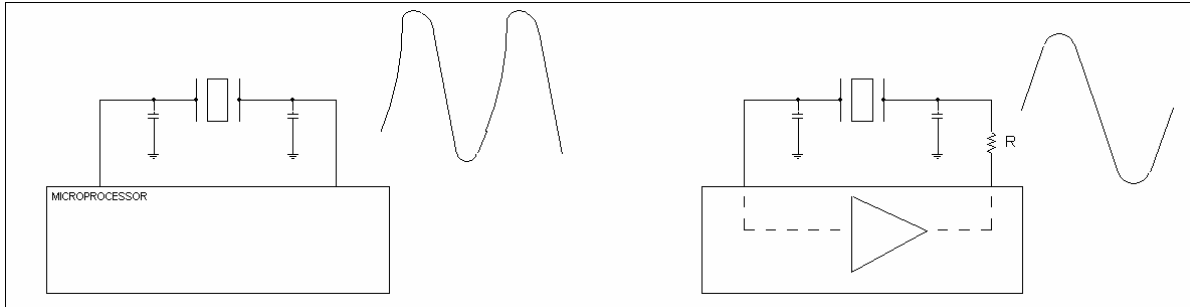
Figure 3.2



#### 4. Crystal, Resonator

- Use SMD components with very short or no trace length to the return plane.
- Begin with 22 - 47 pF capacitors, increase until sinusoidal waveform is achieved. Monitor oscillator signal with active probe (minimum loading). The capacitors may be of different values, typically the driven side (XTAL) is of a higher value.

Figure 4.1



To reduce the oscillator drive current, add resistor R (< 100 ohms).

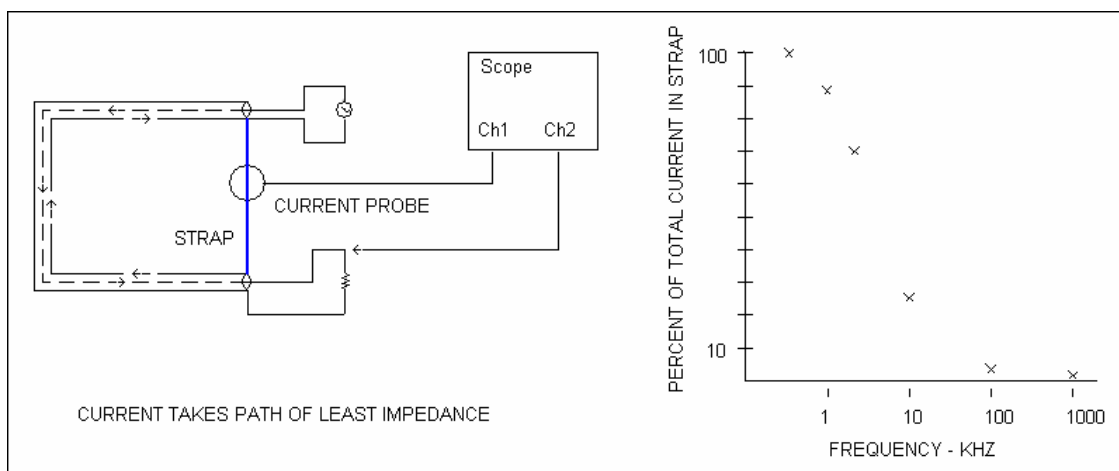
NOTE: For the above oscillator configurations, the IC vendor must be consulted to make sure the circuit is acceptable and starts up at all temperatures.

- Do not run other PCB tracks near crystal/resonator.

#### 5. High Frequency (or fast rise/fall times) Tracks, Components

- At high frequencies, the return currents for a signal track will follow the path of least inductance. See figure 5.1.
- Ground plane under a conductor (track) is ideal for providing this return path.
- Reduces the radiating and pickup loop area (also reduces the track inductance).
- Slots in the PCB which break up this configuration can dramatically reduce the effectiveness of the image plane since the return path will create a larger loop area. See Figure 5.2.
- Use slowest speed IC's consistent with function.

Figure 5.1



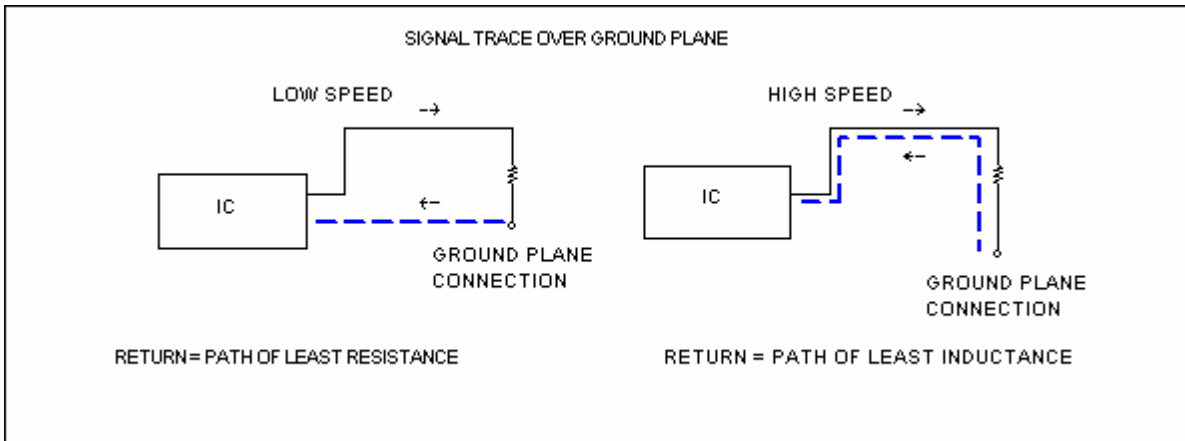
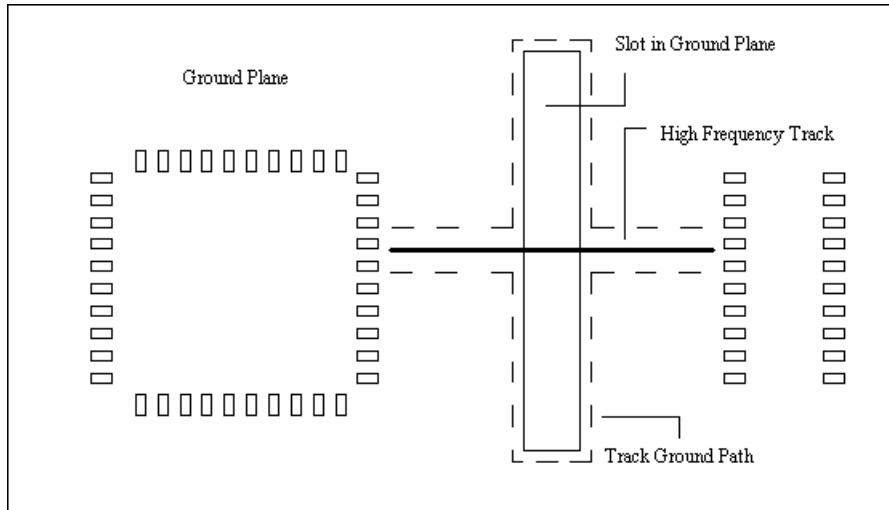
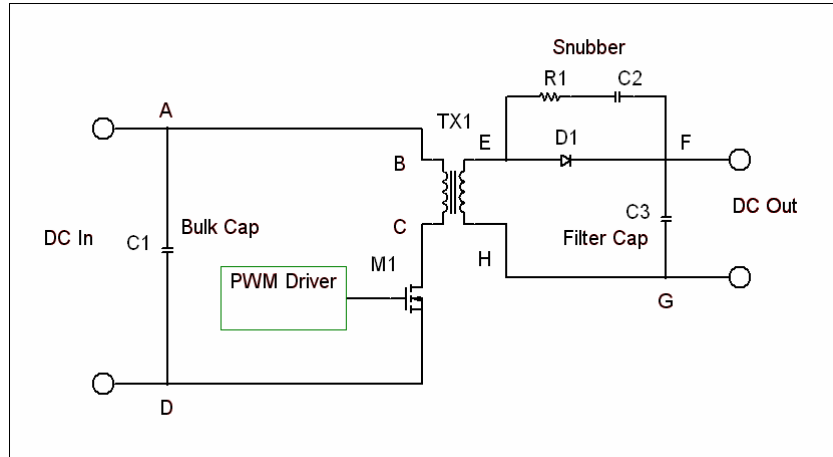


Figure 5.2



## 6. Switching Power Supply:

Figure 6.1



- Use only low ESR capacitors.
- Loop areas A-B-C-D and E-F-G-H must be minimized
- Control edge rates (e.g. add FET gate resistor to slow rise times). Compromise between Radiated Emissions and heat.
- Ground heat sink.
- Verify D1 recovery time is not too fast (soft recovery).
- Reference National Application Note AN-1229.